LOW COST CYCLOCONVERTER INDUCTION MOTOR DRIVES USING NEW MODULATION TECHNIQUES

by Gregory Peter Hunter

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Supervisor: Professor V. S. Ramsden

University of Technology, Sydney
P.O. Box 123, Broadway, N.S.W. 2007
Australia

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CERTIFICATE

I certify that this thesis has not already been submitted for any degree and is not being submitted as part of candidature for any other degree.

I also certify that the thesis has been written by me and that any help that I have received in preparing this thesis, and all sources used, have been acknowledged in this thesis.

Signature of Candidate

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STATEMENT OF ORIGINALITY

All work described in this thesis, except where indicated and acknowledged, is original research undertaken by the author.

The main contributions claimed by the author are as follows:

1. The introduction of the double integral control method for the selection of the thyristor trigger instances in phase controlled naturally commutated cycloconverters. [Section 3.2]

2. The development of a practical algorithm for implementation of the double integral control method in a microprocessor, including the addition of a novel technique for correcting instabilities. [Section 3.3]

3. The development of a simplified algorithm for the double integral control method for use in less demanding applications which can be implemented in a low cost microprocessor. [Section 3.3]

4. The introduction of a new and very accurate method of determining when to change thyristor banks in a circulating current free naturally commutated cycloconverter. [Section 3.4]

5. Use of the above control techniques to develop of a new single phase input to two phase output cycloconverter circuit suitable for driving a split-winding two-phase AC motor which contains only four triacs. [Section 4.1]

6. The presentation of an alternative equivalent circuit for the induction motor valid for arbitrary input waveforms which is useful for an intuitive understanding of induction motor properties. [Chapter 2]

7. The development of a new snubber circuit for the three phase cycloconverter which reduces the size and power dissipation of the snubber components. [Section 5.1]

8. The development of a new gate drive technique for DC excitation of the thyristor gate which takes advantage of the internal gate charge storage of the thyristor. [Section 5.2]

Note on Associated Research

Some research on this topic has also been undertaken by associate J. Zhang [References 26 to 32]. He developed a single phase input to three phase output cycloconverter based on the modulation method described here, developed a full computer simulation of single phase input cycloconverters, investigated the H bridge version of the single phase input to two phase output cycloconverter, and investigated the input harmonics and their impact on the mains of both these single phase input cycloconverters. This work is different to all the above.

ACKNOWLEDGMENTS

The author would like to thank his supervisor, Professor V.S. Ramsden, for his advice, encouragement and support throughout this research project.

The author would also like to thank the staff of the Power and Machines Group in the School for their assistance, particularly in the construction of the cycloconverter prototypes.

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NOMENCLATURE

f_i	input frequency
f_o	wanted output frequency
v_r	output reference voltage
v_o	output voltage
v_t	expected output voltage in the current trigger period after the thyristor is triggered
v_ψ	flux component of the applied motor voltage
i_r	output reference current
i_o	output current
$i_{1\alpha}$	direct axis stator current
$i_{1\beta}$	quadrature axis stator current
$i_{2\alpha}$	direct axis rotor current
$i_{2\beta}$	quadrature axis rotor current
$\lambda_{1\alpha}$	direct axis stator flux linkage
$\lambda_{1\beta}$	quadrature axis stator flux linkage
$\lambda_{2\alpha}$	direct axis rotor flux linkage
$\lambda_{2\beta}$	quadrature axis rotor flux linkage
$e_{1\alpha}$	direct axis stator voltage
$e_{1\beta}$	quadrature axis stator voltage
$e_{2\alpha}$	direct axis rotor voltage

$e_{2\beta}$	quadrature axis rotor voltage
e'_{α}	direct axis back e.m.f.
e'_{β}	quadrature axis back e.m.f.
ω_r	rotor speed in electrical radians per second
L_{11}	per phase stator self inductance
L_{22}	per phase rotor self inductance
L_{12}	per phase mutual inductance between stator and rotor
L_m	per phase magnetising inductance
L_1	per phase stator leakage inductance
L_2	per phase rotor leakage inductance
R_1	per phase stator resistance
R_2	per phase rotor resistance
t_1	start time of a trigger period
t_2	end time of a trigger period
t_f	thyristor trigger time in a trigger period
K	stability constant for double integral control
ψ_t	reference for the flux component of the integral of the motor voltage
p	differential operator

ABSTRACT

This thesis describes new techniques for controlling naturally commutated, circulating current free cycloconverters when used to drive induction motors, then applies these techniques to standard three pulse cycloconverters and to single phase input cycloconverters of new design. A new time domain equivalent circuit of the induction motor for arbitrary input waveforms, which was used in the development of the new control techniques, is also described. The research is a continuation of the author's Masters thesis.

Most aspects of cycloconverters are investigated in detail and improvements in many areas are described. Some examples of these improvements are the development of all digital phase control algorithms that both reduce the cost of the control circuits and improve the performance of the drive, and the development of very low cost cycloconverter drives based on triacs that are suitable for domestic applications. The new digital control algorithms allow a reduction of the number of thyristors required for a 3 phase drive to 18 while at the same time extending the useable upper output frequency limit to one half the mains frequency. The new algorithms also allow, for the first time, an induction motor to be controlled by a single phase input cycloconverter.

The first stage in the research is an investigation of the voltage waveform requirements of the induction motor, including the development of the new time domain equivalent circuit, in order to obtain good motor performance when operating at variable speeds. Rather then using the normal method of looking at the voltage harmonics, the investigation looks at the input voltage waveshape requirements in the time domain. This approach is taken because the extensive harmonic analysis undertaken in the Masters thesis, although showing that improvements could be made in the cycloconverter output waveforms, was of no use in devising control algorithms for making these improvements.

The investigation of the motor requirements shows that it is much more important to control the integral of the applied voltage waveform to the motor than the voltage waveform itself. This information is used to develop the new double integral control algorithm for controlling the phase of the thyristor trigger signals in the cycloconverter. In this algorithm the integral of the cycloconverter output voltage is controlled directly to keep it as close to a reference integral as possible. This algorithm was then refined to improve stability (the algorithm was initially marginally unstable), and to overcome

problems such as bank cross-over determination and operating with discontinuous current. A patent was taken out on the algorithm [25].

The new algorithm is applied to a very low cost, single phase input to 2 phase output cycloconverter driving a 2 phase induction motor which was developed because of the commercial potential of this type of drive and because commercial funding was obtained for its development. The new phase control techniques are also applied to a 3 phase input to 3 phase output, 3-pulse cycloconverter driving an induction motor . An investigation of the resulting input and output waveforms and harmonics is included.

1. INTRODUCTION

1.1 General

This thesis is about naturally commutated cycloconverters (henceforth called just cycloconverters) as used to drive electric motors. The aims are to improve the performance and to lower the cost of the cycloconverter drive.

The research for this thesis is a continuation of the author's Masters thesis completed in 1983 [11]. The Masters thesis investigated the output waveforms and harmonics of the cycloconverter and demonstrated that it should be possible to make improvements in the output harmonic spectrum obtained with traditional phase control techniques such as cosine wave crossing control.

The cycloconverter has been traditionally used only in very high power drives, usually above one megawatt, where no other type of drive can be used. Examples are cement tube mill drives above 5 MW [3,4], the 13 MW German-Dutch wind tunnel fan drive [5], reversible rolling mill drives [6,9] and ship propulsion drives [7,8]. The reasons for this are that the traditional cycloconverter requires a large number of thyristors, at least 36 and usually more for good motor performance, together with a very complex control circuit, and it has some performance limitations, the worst of which is an output frequency limited to about one third the input frequency [10].

This thesis introduces new control techniques which allow good performance to be obtained from drives using low cost, reduced pulse number cycloconverters.

In this chapter, a brief description of cycloconverter motor drives is given with an emphasis on the aspects which are investigated in the thesis. A complete description of the naturally commutated cycloconverter including a thorough investigation of its operation and characteristics can be found in Pelly [10].

In the second chapter, a new transient induction motor equivalent circuit, which is valid for any set of arbitrary input waveforms is developed. This is of assistance in developing the new cycloconverter control techniques.

In the third chapter, the new control method, called double integral control, is described. First a critical appraisal of traditional control methods is given with an emphasis on how they affect the induction motor in the time domain. Next, the new control method

is developed from the requirements of the induction motor in the time domain. Practical implementation for both single and three phase input cycloconverters, including ways of dealing with discontinuous current and bank cross-over determination, is then described.

In the remaining fourth and fifth chapters, two cycloconverter drives using the new control techniques are described. These are a single phase input cycloconverter driving a two phase induction motor and a three phase input cycloconverter driving a three phase induction motor. The results of performance tests on these drives are also presented.

1.2 The Single Phase Input Cycloconverter

The circuit of a single phase input to single phase output cycloconverter is shown in Figure 1.1. It is perhaps the simplest type of cycloconverter and will be used in this thesis as the basis for the investigations into the operation of the cycloconverter and for developing techniques for improving its performance. It is classed as a 2-pulse cycloconverter because there are two phase controlled pulses per mains cycle per output phase [10]. If more than one output phase is needed, the single phase output circuit is just duplicated to create the extra phases. If a neutral return is not required in a multiphase output application, the transformer can be removed to simplify the circuit.

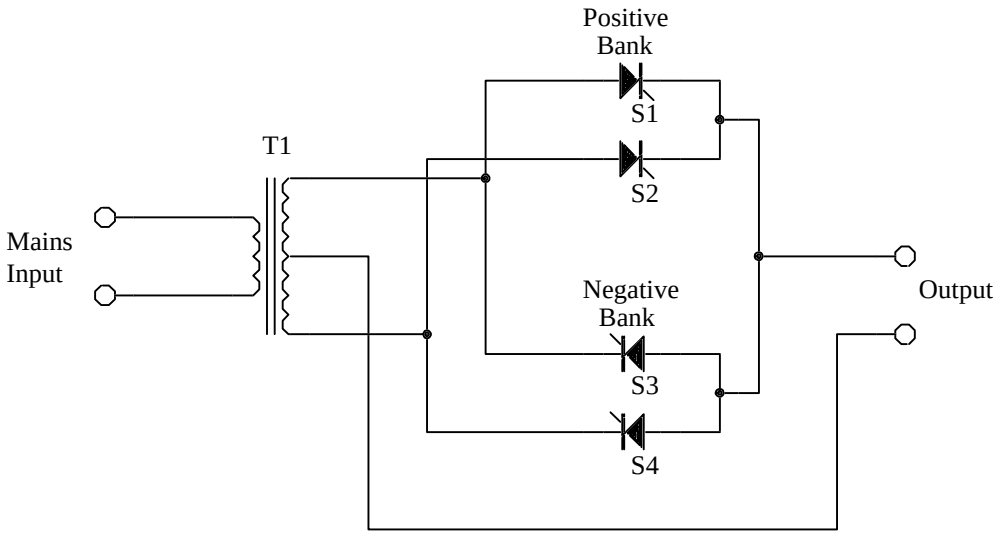
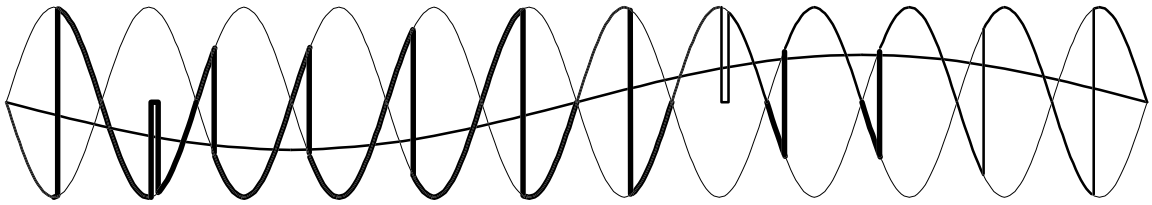


Figure 1.1 Basic single phase cycloconverter.

The cycloconverter has four thyristors divided into a positive and negative bank of two thyristors each. When positive current flows in the load, the output voltage is controlled by phase control of the two positive bank thyristors whilst the negative bank



Input, Output and Reference Voltages

Output Current

Figure 1.2 Idealised waveforms for a 2-pulse cycloconverter with 45° lagging load current.

thyristors are kept off and vice versa when negative current flows in the load. An idealised output waveform for a sinusoidal load current and a 45 degrees load phase angle is shown in Figure 1.2.

It is important to keep the non conducting thyristor bank off at all times, otherwise the mains could be shorted via the two thyristor banks, resulting in waveform distortion and possible device failure from the shorting current. A major control problem of the cycloconverter is how to swap between banks in the shortest possible time to avoid distortion whilst ensuring the two banks do not conduct at the same time.

A common addition to the power circuit that removes the requirement to keep one bank off is to place a centre tapped inductor called a circulating current inductor between the outputs of the two banks as shown in Figure 1.3. Both banks can now conduct together without shorting the mains. Also, the circulating current in the inductor keeps both banks operating all the time, resulting in improved output waveforms. This technique is not often used, though, because the circulating current inductor tends to be expensive and bulky and the circulating current reduces the power factor on the input (although one paper [12] has suggested using a controlled circulating current together with input capacitors to actually improve the input power factor).

This thesis is concerned only with cycloconverters without circulating current inductors, called circulating current free cycloconverters. No further mention will be made of circulating current type cycloconverters, although the phase control modulation methods developed for this thesis could be applied to advantage to this type of cycloconverter.

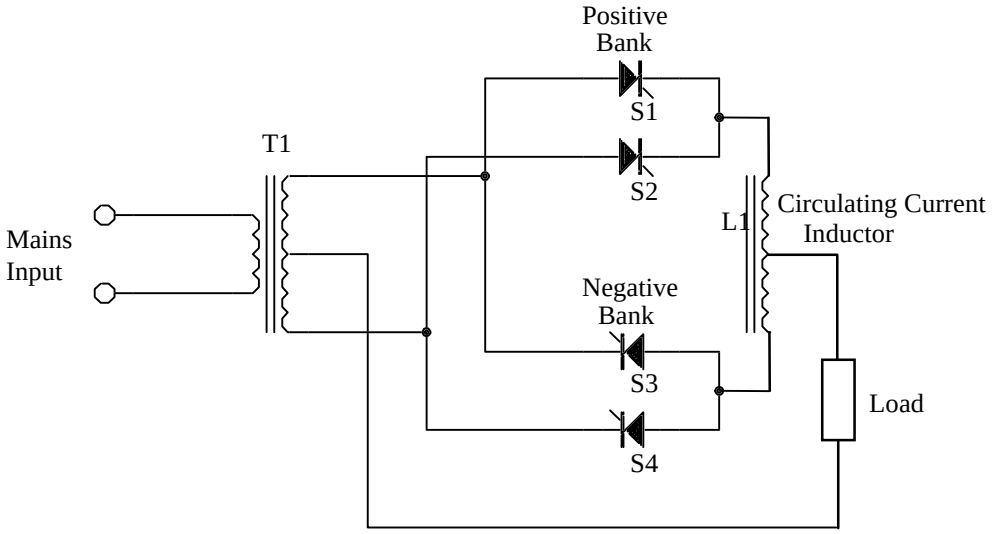


Figure 1.3 Two-pulse cycloconverter with circulating current inductor.

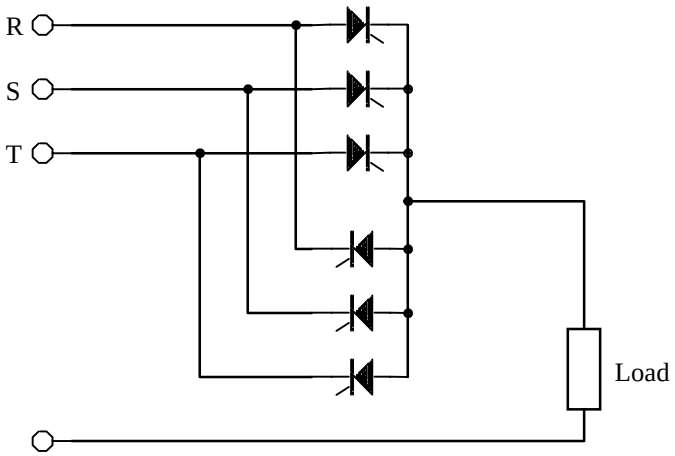


Figure 1.4 Three phase, 3-pulse cycloconverter.

1.3 The Three Phase Input Cycloconverter

The circuit of a three pulse, three phase input to one phase output cycloconverter is shown in Figure 1.4. Its operation is identical to that of the single phase cycloconverter of Figure 1.1, except that there are now three AC inputs phase shifted by 120° instead of two AC inputs phase shifted by 180°. An example of an idealised output waveform for a 45° load phase angle where the output load current is sinusoidal is shown in Figure 1.5.

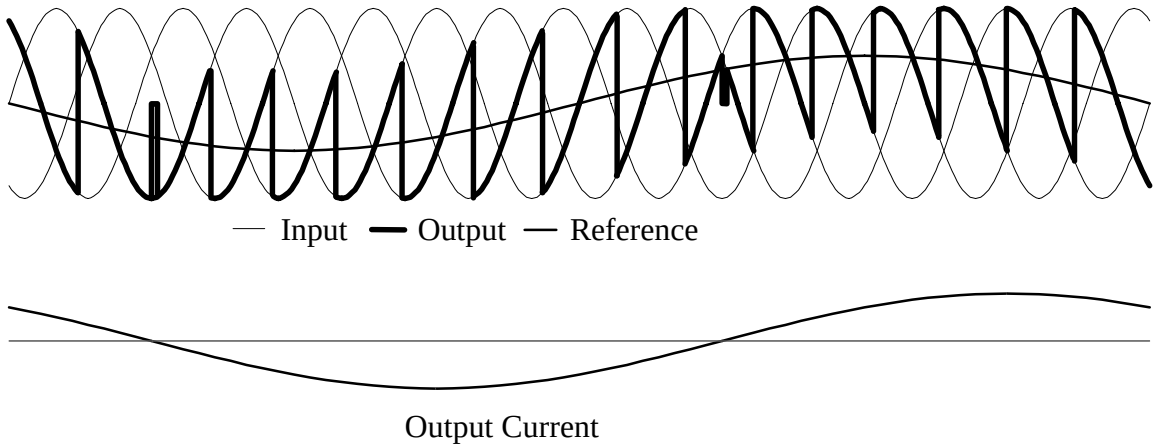


Figure 1.5 Idealised waveforms for a 3-pulse cycloconverter with 45° lagging load current.

The three phase input, 3-pulse cycloconverter can be effectively extended to a 6 phase input cycloconverter by using a bridge circuit of 12 thyristors for each output phase as shown in Figure 1.6. This is called a 3 phase input, 6-pulse cycloconverter because there are now 6 phase controlled pulses on the output per mains input cycle. This circuit gives much lower input and output current harmonics at the expense of double the number of thyristors and a more complex control circuit. Another disadvantage is that when three such circuits are combined to create a three phase output cycloconverter, the inputs to each of the three circuits must be galvanically isolated from each other using transformers if the outputs are to be connected into a three phase, 3 wire configuration, as is required for a 3 phase motor. Despite this disadvantage, this is the minimum configuration used in commercial cycloconverters (for example [4,8]). Pelly [10] has suggested using a motor with 3 isolated phases to avoid a transformer but this is never used in practice, probably because this results in a very low impedance being presented to any zero sequence harmonics that may appear on the cycloconverter outputs.

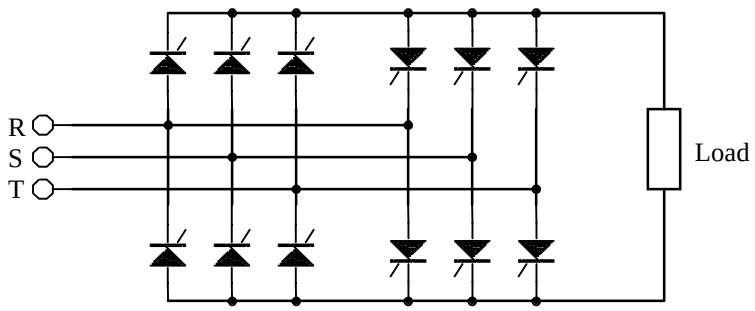


Figure 1.6 Three phase input, 6-pulse cycloconverter.

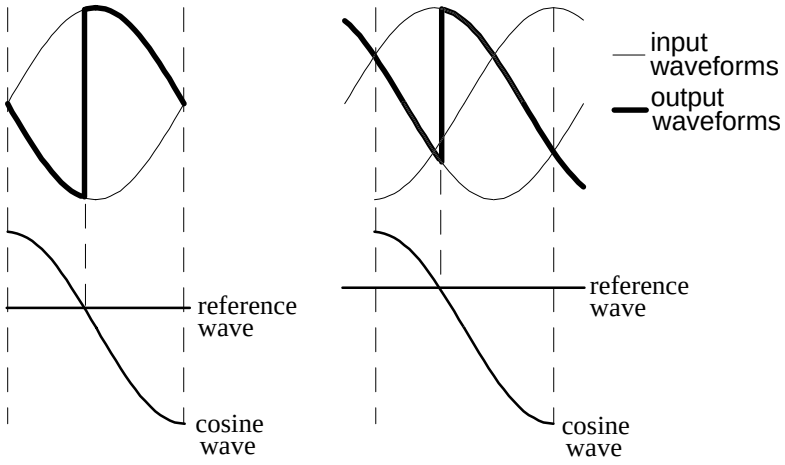
As part of the work for this thesis, a three phase input to three phase output, 3-pulse cycloconverter based on the circuit of Figure 1.4 is developed. This work is described in Chapter 5.

1.4 Phase Control Methods

Of various phase control methods developed in the past, only one, cosine wave crossing control, has found widespread use and this is described below. Another method that has been reported which is of interest because it is related to the double integral phase control method developed in this thesis is integral control. This is also described below. Both methods are described in detail by Pelly[10].

1.4.1 Cosine Wave Crossing Control

In the cosine wave crossing control method, the output reference wave is compared with cosine waves and when the two waveforms cross, the thyristors are triggered. The procedure is shown in Figure 1.7 for both 2-pulse and 3-pulse cycloconverters.



(a) Two-pulse cycloconverter (b) Three pulse-cycloconverter

Figure 1.7 Cosine wave crossing phase control method. Illustrated for positive load current.

The cosine wave crossing control method was originally developed for DC output thyristor converters. For this application, the method produces an average output voltage which is directly proportional to the reference voltage for the idealised case of continuous output current. Pelly[10] showed that when applied to the idealised (continuous output current) cycloconverter, this method produces an output voltage

whose fundamental component amplitude is proportional to the reference waveform amplitude and whose frequency spectrum contains no multiples of the fundamental component.

Even though the cosine wave crossing control method is almost universally used for cycloconverter motor drives, the method has some severe limitations when used in this application. The main limitation is that the method generates intermodulation products on the output, the frequency of which may be less than the wanted output frequency. When this occurs, the intermodulation product is called a subharmonic.

For example, consider a 3-pulse cycloconverter which has an input frequency, f_i, of 50 Hz and a fundamental output frequency, f_o , of 24 Hz. This can generate intermodulation products of frequencies $(3nf_i + mf_o)$ where *n* and *m* are integers. The intermodulation product, $(3f_i - 6f_o)$, has a frequency of 6 Hz which is less than f_o and is thus a subharmonic. For cosine wave crossing control, assuming maximum output modulation and a load phase angle of 30° lagging, its amplitude is 9.5% of the fundamental [10,11]. For an induction motor operating at a synchronous speed of 24 Hz, its impedance at 6 Hz would be very low and the currents and resulting torque pulsations produced from this subharmonic would be unacceptably high.

Another major problem with cosine wave crossing control is the distortion produced from discontinuous output current. When the motor is operating under light load, the high ripple current may bring the output current in a phase to zero, turning off the conducting thyristor before the next thyristor turns on. The output voltage will then revert to the motor open circuit voltage rather than the input phase voltage, causing considerable voltage distortion on the output. For a 2-pulse cycloconverter with an induction motor load, as will be shown later in this dissertation, the ripple current is so large that the current drops to zero during the conduction of every thyristor even under full load. Cosine wave crossing control is not viable in this situation.

1.4.2 Correction Methods for Cosine Wave Crossing Control

There have been various techniques devised over the years to correct the deficiencies of the cosine wave crossing control method. Most commercial drives use one of these techniques. The important ones are described below.

1.4.2.1 Regular Sampling

The regular sampling method was developed by Bird and Ford [13] for circulating current cycloconverters. The method is to modify the reference waveform by doing a sample and hold at the start of each cosine wave. This was found to reduce the amplitudes of subharmonics on the output. Further work by the author [11] showed that identical and improved results could be obtained by pre-distorting the reference wave. This work also showed that this technique provides minimal improvement for circulating current free cycloconverters.

1.4.2.2 Ripple Voltage Integral Feedback

Ripple voltage integral feedback is a technique introduced by Gyugyi and Pelly [14]. It involves feeding back the integral of the difference between the output voltage and the reference voltage. A block diagram of this scheme is shown in Figure 1.8. With this system, any low frequency subharmonics are attenuated by the feedback, the gain of which is inversely proportional to frequency. The feedback would also assist in reducing voltage distortion due to discontinuous current.

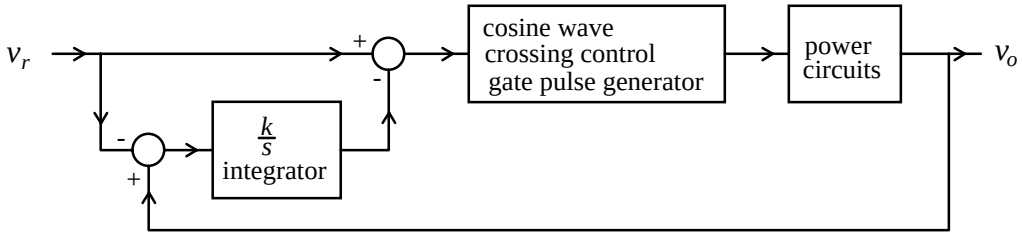


Figure 1.8 Simplified block diagram of ripple voltage integral feedback control scheme.

The limitation of this technique is that the maximum stable loop gain is rather low and is reduced as the maximum output frequency is increased. Table 1.1 shows the approximate maximum stable unity gain frequency of the feedback loop for a 50 Hz input frequency, 3-pulse cycloconverter for various output frequencies. This table is constructed from data presented by Gyugyi and Pelly [14].

Table 1.1 Approximate maximum stable unit gain frequency of the feedback loop for a 50 Hz input frequency, 3-pulse cycloconverter

Output Frequency (Hz)	Unity Gain Frequency (Hz)
5.56	9.5
8.33	7
16.67	5.5
25	4.5
33.33	3.5

Note that for a 3-pulse cycloconverter operating up to 25 Hz, the feedback gain is quite low and of limited benefit. Assuming that the loop gain drops off by 20 dB per decade, then at 6 Hz, the maximum gain is only 0.75, producing only a marginal reduction in a subharmonic at this frequency. A way of increasing the maximum stable unity gain frequency is to increase the pulse number. For a 6-pulse cycloconverter, the maximum unity gain frequency can be multiplied by 4, and for 12-pulse, by 16. Gyugyi and Pelly [14] demonstrated good results using this system for a 6-pulse cycloconverter operating up to 2/3 of the input frequency and driving a 30 HP induction motor.

1.4.2.3 Current Feedback

The most common commercial method of improving the output waveform is feedback of the output current. This method evolved from its use in thyristor controlled DC motor drives. A block diagram of current feedback control is shown in Figure 1.9.

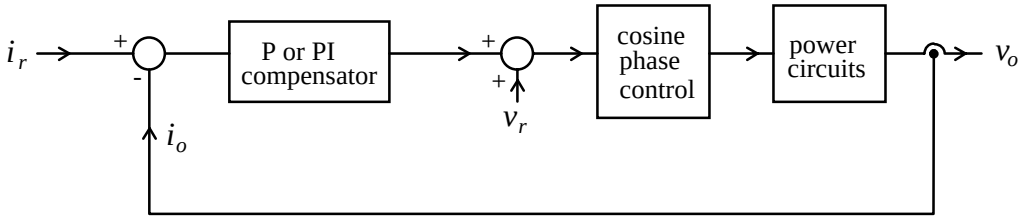


Figure 1.9 Simplified block diagram of current feedback control scheme.

In terms of feedback stability and gain, the current feedback system is virtually identical to ripple voltage integral feedback. The approximate equivalent circuit of the motor is a back e.m.f. in series with a leakage inductance, so the current signal is proportional to the integral of the output voltage minus the back e.m.f. which is approximately equal to the wanted reference voltage. This means that the maximum feedback gain without instability is similar to that which can be obtained from ripple voltage integral feedback. This limits the usefulness of current feedback to 6-pulse and higher cycloconverters. Even with 6-pulse cycloconverters, an estimate of the wanted output voltage must be added to the error voltage as shown in Figure 1.9 to reduce the error in the output current.

Although there is little difference in performance between ripple voltage integral feedback and current feedback, current feedback is usually chosen in practice because it allows easier implementation of vector control.

Some commercial examples of cycloconverter drives using cosine wave crossing control and current feedback, and always with vector control added, are described in references [3,4,5,6,8].

1.4.3 Integral Control

Integral control is a seldom used method of phase control for the cycloconverter which was invented by Gyugyi, Rosa and Pelly [15,10]. It is of interest here because it is in the same class of phase control schemes as the double integral phase control method developed in this thesis.

The basic method is to trigger the next thyristor when the integral of the difference between the reference and the output voltage waveforms reaches zero. A block diagram of an integral control system is shown in Figure 1.10. The difference between the reference voltage and the output voltage is fed to an integrator, the output of which is connected to a zero detector. The zero detector is used to advance a ring counter which

turns on each thyristor in sequence in the conducting bank. The same circuit, or computer algorithm if implemented in software, can be used for both the positive and negative bank by reconnecting the outputs of the ring counter to the appropriate thyristors. The relevant waveforms for positive and negative load current for a 2-pulse cycloconverter are shown in Figure 1.11.

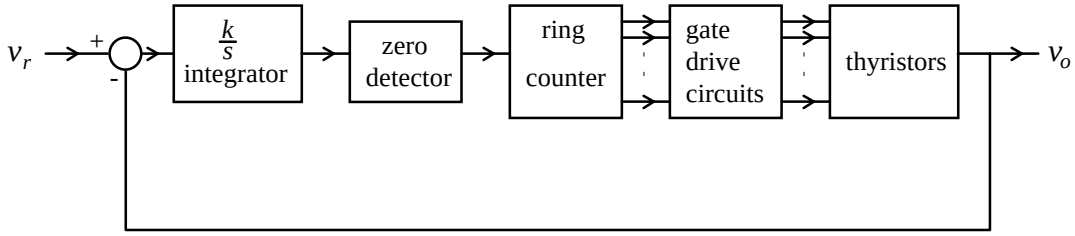
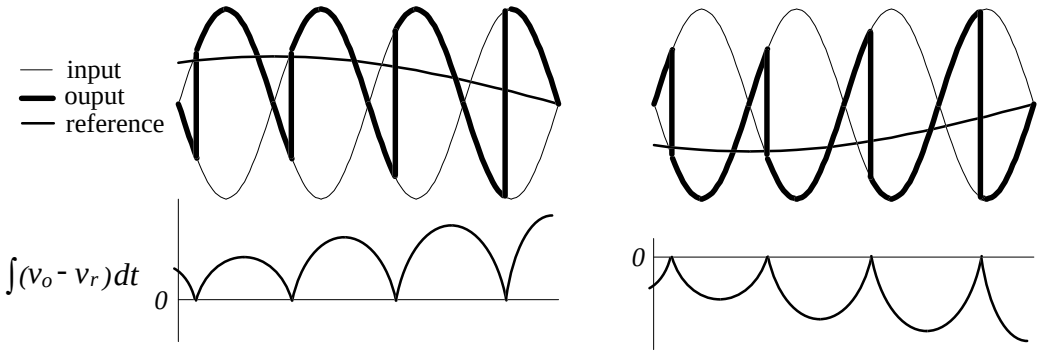


Figure 1.10 Block diagram of integral control.



(a) Positive bank operation (b) Negative bank operation

Figure 1.11 Waveforms obtained from a 2-pulse cycloconverter with integral control.

A problem with the basic integral control method is that it can exhibit instability, an example of which is shown in Figure 1.12. Several methods have been developed to suppress the instability without upsetting the integral control action [15,16,17]. These methods will not be described here, but they are fairly easy to implement.

1.4.4 Pre-integral Control

Pre-integral control is an interesting variation of integral control developed by the author [11] but never implemented. It was developed for the 3-pulse cycloconverter but can be applied to cycloconverters of any pulse number. Its operation is shown in Figure 1.13. For each output phase, the output waveform is divided into periods called trigger periods, each of which contains only one thyristor switching instance. Each trigger period starts when the reference waveform crosses the input waveform which is

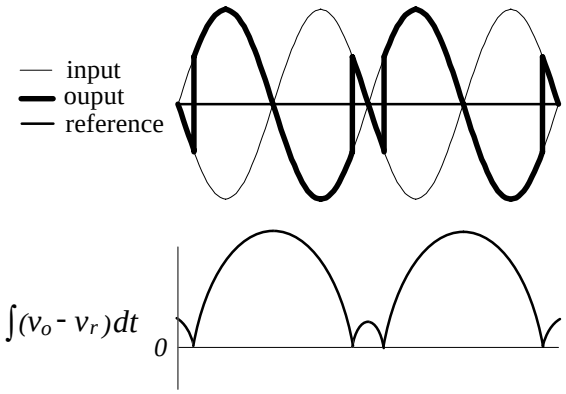


Figure 1.12 An example of instability for a 2-pulse cycloconverter with integral control.

currently connected to the output and ends when the reference waveform crosses the input waveform connected to the next thyristor to be turned on. These start and end times are chosen because these are the limits within which the thyristor will always turn on. The thyristor is triggered on when it is estimated by computer calculation that the integral of the difference between the output and reference waveforms will be zero at the end of the current trigger period.

The advantage of pre-integral control over integral control is that it is inherently stable. The disadvantage is that a microprocessor is required to calculate the difference integral in advance. If the output current is discontinuous, resulting in the thyristor that is on at the start of the trigger period turning off before the next thyristor turns on, as shown in Figure 1.14, then the microprocessor must continually recalculate the turn-on time of the next thyristor up to when the thyristor is turned on because with no thyristor conducting, the output voltage cannot be determined in advance.

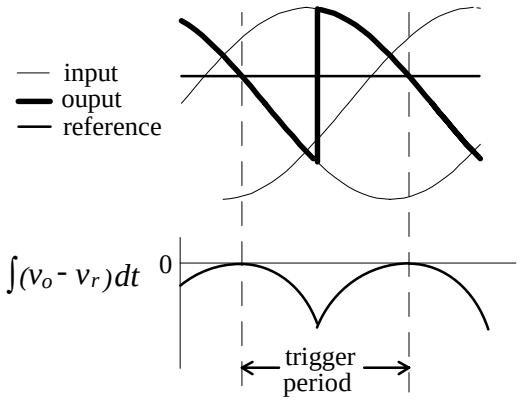


Figure 1.13. Illustration of the pre-integral control method for positive load current.

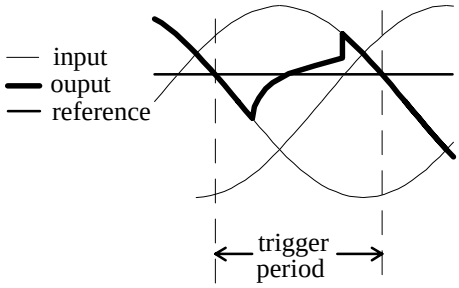


Figure 1.14 Pre-integral control with discontinuous current.

1.5 The Bank Cross-Over Problem

A major problem with the circulating current free cycloconverter is the selection of the time to cross over from one bank to the other. With ideal sinusoidal load current, the bank can be switched when the current goes to zero. With a typical load, though, and especially an induction motor load which has low series inductance, the ripple current is significant and can result in the instantaneous current going to zero long before the fundamental component of the current reaches zero.

With 3 phase input to 3 phase output cycloconverters, where only moderate ripple current occurs, several practical solutions have been devised. With a vector controlled motor drive with an inner current feedback loop as is shown in Figure 1.9, the usual solution is to just change banks when the reference current, i_r, goes through zero.

With an open loop voltage control scheme using cosine wave crossing control, the usual method is to switch banks at the first current zero [10]. A refinement for lagging power factor loads such as an induction motor is to also require the condition that the reference voltage must be of opposite polarity to the bank direction [18]. These methods usually result in premature bank switching causing added voltage distortion, but are reliable and simple to implement.

No method for determining the bank cross-over time for integral control has been found in the literature, with all practical examples of integral control being applied to circulating current cycloconverters. The first current zero method could possibly also be used here.

For a single phase input cycloconverter, the problem of determining the bank cross-over time is much worse because the ripple current with an induction motor load is large

enough to bring the instantaneous output current to zero at nearly every half cycle, even at full load (for example, see Figure 4.16).

1.6 Recent Research

This chapter has summarised the phase control techniques available for cycloconverters at present. It has been shown that there are many problems with the current techniques and more research is required to solve these. Unfortunately, apart from the work undertaken by the author and his associates, there is very little research being undertaken in this area at present.

The last published results of research into alternative phase control techniques to cosine wave crossing control was by Pelly [10] in 1971. Since then, there has only been attempts to add modifications to the cosine wave crossing control technique to reduce its problems. Bird and Ford, 1974 [13] added regular sampling and found that this reduced the level of sub-harmonics for circulating current cycloconverters. Unfortunately, later research by this author [11] has shown that the improvements obtained for circulating current free cycloconverters using this technique is minimal. Nevertheless, this addition is usually incorporated in modern digitally controlled cycloconverters because it makes the digital implementation of cosine wave crossing control much simpler. A more recent attempt to improve on cosine wave crossing control was made by Juby et al, 1995 [20]. For a cycloconverter proposed for naval propulsion systems, the low frequency harmonics generated by the cycloconverter using cosine wave crossing control can excite mechanical resonances causing unwanted water borne noise. The authors proposed cancelling out harmonics at specific troublesome frequencies by adding the harmonics in anti-phase to the sinusoidal reference waveforms. This is a rather complicated way of solving the problems caused by the use of the non-ideal cosine wave crossing control method.

The author believes that the reason why no significant research into phase control techniques have been conducted since Pelly, 1971 [10], is that there is a general belief, first expressed by Pelly, that cosine wave crossing control cannot be improved on. For example, in a recent paper by Arsov, 1994 [21], it is stated: “In the case of analog control, the cosine wave crossing principle is known as the most natural one, also having the property to produce minimum possible total distortion of the output voltage waveform.”, citing Pelly as the source for this result. This thesis will show that this belief is incorrect and that much better phase control methods can be developed.

2. AN INDUCTION MOTOR EQUIVALENT CIRCUIT FOR ARBITRARY INPUT WAVEFORMS

2.1 Introduction

The main aim of this thesis is to develop improved phase control methods for a cycloconverter when used to drive an induction motor. The method used is to investigate the cycloconverter and the motor in the time domain. This chapter introduces a new time domain equivalent circuit for the induction motor valid for any arbitrary input waveforms [23]. This equivalent circuit is used to gain an intuitive understanding of the basic properties of the input waveforms that are required to drive the induction motor. This is of assistance in the development of the improved cycloconverter phase control methods in the following chapters. The equivalent circuit can also be used directly in circuit simulation packages such as SPICE. Unlike mathematical models, using this equivalent circuit model gives easy access to inner motor quantities such as flux and magnetising current.

A literature survey has found no such equivalent circuit valid for arbitrary input waveforms. Only mathematical time domain models suitable for computer simulations, or equivalent circuits that include some element of the frequency domain (such as the classic steady state equivalent circuit) have been reported.

The chapter stands alone in that a knowledge of the equivalent circuit developed is not required to understand the following chapters on cycloconverter phase control techniques, provided the reader has a basic understanding of the induction motor properties. Also, the equivalent circuit developed has more general applications than just as an aid to developing new phase control methods for the cycloconverter.

In the chapter, the equivalent circuit for the basic two phase, two pole, squirrel cage motor is first developed. This is then extended to an equivalent circuit for the three phase induction motor.

2.2 Assumptions

In this derivation of a time domain equivalent circuit, the following assumptions have been made:

1. Saturation, hysteresis and eddy current effects are ignored.

2. The windings are effectively sinusoidally distributed and the effects of teeth and slots are ignored, i.e. with DC excitation, the space m.m.f. is sinusoidally distributed.

3. For the three phase version of the equivalent circuit, there is no neutral connection.

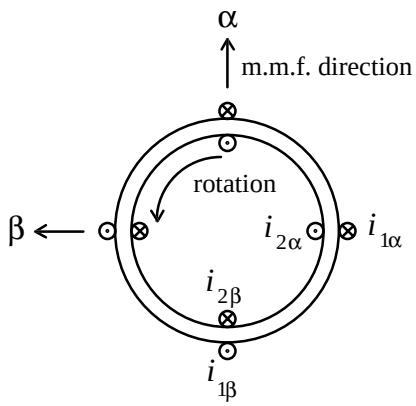


Figure 2.1 Basic two phase induction motor.

2.3 Derivation of the Equivalent Circuit

2.3.1 Motor Configuration

For ease of development, a two phase in quadrature, two pole representation of the induction motor is used. Let the two phases be called the α and β phases and the direction of the m.m.f.'s generated by these two phases the α and β axes. This basic machine is shown in Figure 2.1. As seen in this diagram, the stator currents are $i_{1\alpha}$ and $i_{1\beta}$ and the rotor currents are $i_{2\alpha}$ and $i_{2\beta}$. The reference directions of the rotor currents are reversed to those of the stator currents to correspond to the actual direction of the currents in a machine. This makes it easy to see the correspondence between the model and a real machine. To simplify the equations, it is assumed that all windings have the same number of turns.

2.3.2 Flux Linkages

The rotor and stator axes are stationary and the rotor has no saliency so the self and mutual inductances are constant. Also the α and β axes are in quadrature so there are no flux linkages between the two axes. As well, because the α and β windings are

identical, they have identical inductance values. Using this information, and representing the flux linkages by λ, the flux linkage equations are:

Stator:

$$\lambda_{1\alpha} = L_{11} i_{1\alpha} - L_{12} i_{2\alpha} \tag{2.1}$$

$$\lambda_{1\beta} = L_{11} i_{1\beta} - L_{12} i_{2\beta} \tag{2.2}$$

Rotor:

$$\lambda_{2\alpha} = -L_{22} i_{2\alpha} + L_{12} i_{1\alpha} \tag{2.3}$$

$$\lambda_{2\beta} = -L_{22} i_{2\beta} + L_{12} i_{1\beta} \tag{2.4}$$

Let $L_{12} = L_m$, $L_{11} = L_m + L_1$, $L_{22} = L_m + L_2$, $i_{1\alpha} - i_{2\alpha} = i_{m\alpha}$, and $i_{1\beta} - i_{2\beta} = i_{m\beta}$. As will be shown later, L_m, L_1 and L_2 are the magnetising, stator leakage and rotor leakage inductances respectively and $i_{m\alpha}$ and $i_{m\beta}$ are the α and β phase magnetising currents. The effect of the spatial variation in mutual inductance between the stator and rotor is not included here and is instead accounted for by the normal method of introducing a speed voltage in the voltage equations below. Insert these parameter changes into equations 2.1 to 2.4 to produce equations 2.5 to 2.8:

Stator:

$$\lambda_{1\alpha} = L_1 i_{1\alpha} + L_m i_{m\alpha} \tag{2.5}$$

$$\lambda_{1\beta} = L_1 i_{1\beta} + L_m i_{m\beta} \tag{2.6}$$

Rotor:

$$\lambda_{2\alpha} = -L_2 i_{2\alpha} + L_m i_{m\alpha} \tag{2.7}$$

$$\lambda_{2\beta} = -L_2 i_{2\beta} + L_m i_{m\beta} \tag{2.8}$$

2.3.3 Voltages

The voltage on each stator winding has two components: the IR drop and the voltage due to the rate of change of flux. Each rotor winding has these two components plus a "speed" voltage due to the movement of the rotor conductors through the magnetic field. The stator and rotor voltages, denoted by e , are given by the equations:

Stator:

$$e_{1\alpha} = R_1 i_{1\alpha} + p\lambda_{1\alpha} \tag{2.9}$$

$$e_{1\beta} = R_1 i_{1\beta} + p\lambda_{1\beta} \tag{2.10}$$

Rotor:

$$e_{2\alpha} = -R_2 i_{2\alpha} + p\lambda_{2\alpha} - \lambda_{2\beta}\omega_r \tag{2.11}$$

$$e_{2\beta} = -R_2 i_{2\beta} + p\lambda_{2\beta} + \lambda_{2\alpha}\omega_r \tag{2.12}$$

R_1 and R_2 are the stator and rotor winding resistances, p is the differential operator and ω_r is the rotor speed in electrical radians per second.

It is assumed here the motor is a squirrel cage induction motor which has no external voltage applied to the rotor, so $e_{2\alpha}$ and $e_{2\beta}$ are zero. Equations 2.11 and 2.12 then become:

Rotor:

$$R_2 i_{2\alpha} = p\lambda_{2\alpha} - \lambda_{2\beta}\omega_r \tag{2.13}$$

$$R_2 i_{2\beta} = p\lambda_{2\beta} + \lambda_{2\alpha}\omega_r \tag{2.14}$$

2.3.4 Equivalent Circuit

Using equations 2.5 to 2.10, 2.13 and 2.14 , an equivalent circuit of the induction motor can be derived.

Taking the α phase, combine equations 2.5 and 2.9 to eliminate the flux linkage term $\lambda_{1\alpha}$, giving the equation:

$$e_{1\alpha} = R_1 i_{1\alpha} + L_1 p i_{1\alpha} + L_m p i_{m\alpha} \tag{2.15}$$

This equation, together with the previously defined relation $i_{1\alpha} - i_{2\alpha} = i_{m\alpha}$, can be represented by the equivalent circuit of Figure 2.2. The impedance *Z* in this circuit is as yet unknown. To find this impedance, expand the term $L_m p i_{m\alpha}$ in equation 2.15 using equations 2.7 and 2.13 combined to eliminate the flux linkage term $\lambda_{2\alpha}$. This gives the equation:

$$L_m p i_{m\alpha} = L_2 p i_{2\alpha} + R_2 i_{2\alpha} + \lambda_{2\beta}\omega_r \tag{2.16}$$

Using this equation, the equivalent circuit of Figure 2.2 can be expanded to that of Figure 2.3. Repeating the above derivation for the β phase, the equivalent circuit of Figure 2.4 is obtained.

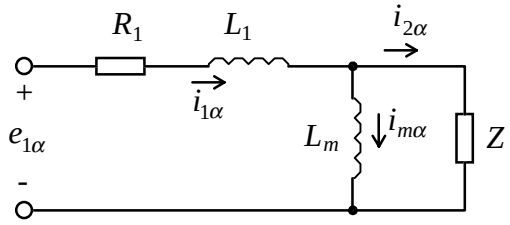


Figure 2.2 Partial equivalent circuit of the α phase.

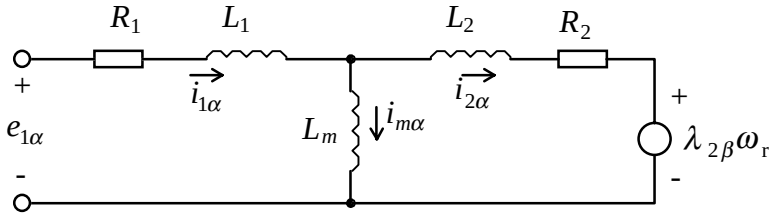


Figure 2.3 Equivalent circuit for the α phase.

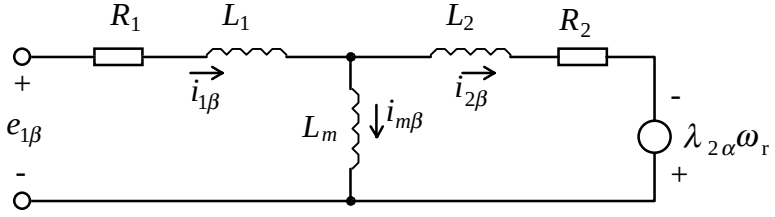


Figure 2.4 Equivalent circuit of the β phase.

All that remains now is to expand the speed voltage terms $\omega_r\lambda_{2\alpha}$ and $\omega_r\lambda_{2\beta}$. Taking $\omega_r\lambda_{2\beta}$ as an example, then from equation 2.8:

$$\begin{aligned}\lambda_{2\beta} &= -L_2 i_{2\beta} + L_m i_{m\beta} \\ &= \int \left(L_m p i_{m\beta} - L_2 p i_{2\beta} \right) dt \\ &= \int e'_\beta dt\end{aligned} \tag{2.17}$$

where $e'_\beta = L_m p i_{m\beta} - L_2 p i_{2\beta}$ and $\int$ is the integral from a time when all currents were zero to time t. This places e'_β as the voltage across L_m and L_2 in the equivalent circuit for the β phase in Figure 2.4.

Using equation 2.17 and the equivalent equation for $\lambda_{2\alpha}$, the equivalent circuits of Figures 2.3 and 2.4 can be expanded into the final equivalent circuit of the two phase induction motor shown in Figure 2.5.

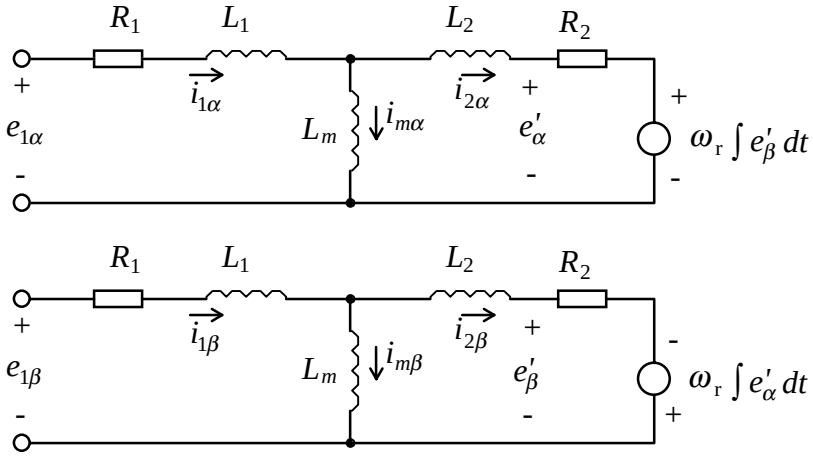


Figure 2.5 Final equivalent circuit of the two phase induction motor.

2.3.5 Derivation of Kron's Equations

The general two-axes equations of the induction motor with the reference frame attached to the stator are known as Kron's equations after Gabriel Kron, the developer of the two axes theory of electrical machines and are presented by Adkins in his general theory of electrical machines[1]. The equations relate the stator and rotor voltages and currents in the direct and quadrature axes of the basic induction motor of Figure 2.1.

The relevant version of the two phase equivalent circuit, with the voltages and currents to be related indicated, is shown in Figure 2.6. Externally applied rotor voltages, $e_{2\alpha}$ and $e_{2\beta}$, have been added to the equivalent circuit to make it more general.

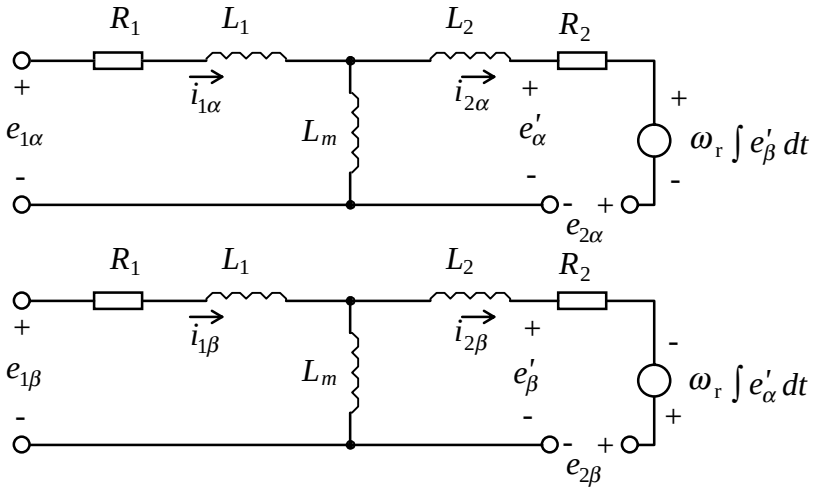


Figure 2.6 Equivalent circuit of the two phase induction motor with rotor voltages added for derivation of Kron's Equations.

From the equivalent circuit, letting $L_{11} = L_1 + L_m$, the stator loop equations are:

$$e_{1\alpha} = (R_1 + L_{11}p)i_{1\alpha} - L_m p i_{2\alpha} \tag{2.18}$$

$$e_{1\beta} = (R_1 + L_{11}p)i_{1\beta} - L_m p i_{2\beta} \tag{2.19}$$

Letting $L_{22} = L_2 + L_m$, the rotor loop equations are:

$$\begin{aligned} e_{2\alpha} &= L_m p i_{1\alpha} - (R_2 + L_{22}p)i_{2\alpha} - \omega_r \int e'_\beta dt \\ &= L_m p i_{1\alpha} - (R_2 + L_{22}p)i_{2\alpha} + \omega_r L_{22} i_{2\beta} - \omega_r L_m i_{1\beta} \end{aligned} \tag{2.20}$$

$$\begin{aligned} e_{2\beta} &= L_m p i_{1\beta} - (R_2 + L_{22}p)i_{2\beta} + \omega_r \int e'_\alpha dt \\ &= L_m p i_{1\beta} - (R_2 + L_{22}p)i_{2\beta} - \omega_r L_{22} i_{2\alpha} + \omega_r L_m i_{1\alpha} \end{aligned} \tag{2.21}$$

Equations 2.18 to 2.21 are Kron's equations. They can be rearranged in the normal matrix form as follows.

$$\begin{bmatrix} e_{1\alpha} \\ e_{1\beta} \\ e_{2\alpha} \\ e_{2\beta} \end{bmatrix} = \begin{bmatrix} R_1 + L_{11}p & 0 & L_m p & 0 \\ 0 & R_1 + L_{11}p & 0 & L_m p \\ L_m p & -\omega_r L_m & R_2 + L_{22}p & -\omega_r L_{22} \\ \omega_r L_m & L_m p & \omega_r L_{22} & R_2 + L_{22}p \end{bmatrix} \begin{bmatrix} i_{1\alpha} \\ i_{1\beta} \\ -i_{2\alpha} \\ -i_{2\beta} \end{bmatrix} \tag{2.22}$$

The rotor currents have been reversed in sign to match the convention used by Adkins.

Note that the equivalent circuit and Kron's equations are closely related in that the equations can almost be "read" directly from the equivalent circuit. Alternatively, the equivalent circuit could be considered as a visual understanding of Kron's equations. The equivalent circuit, though, offers insights not available from inspection of the equations, such as allowing a rough estimate of the motor terminal voltage following the open circuiting of the windings, or getting a feel for the factors influencing the rotor flux linkage, represented by $\int e'_\alpha dt$ and $\int e'_\beta dt$.

2.3.6 Two Phase to Three Phase Conversion

The two phase equivalent circuit derived in Section 2.3.4 can be converted to a three phase equivalent circuit provided there is no neutral connection to the three phase circuit (i.e. there are no zero sequence components). The derivation of the three phase equivalent circuit is as follows:

Let the three stator phases be *a*, *b* and *c*. Let the axis of the α phase in the direct-quadrature representation correspond to the axis of the *a* phase. The relative location of the two sets of axes as they would appear on the basic two pole motor of Figure 2.1 are shown in Figure 2.7.

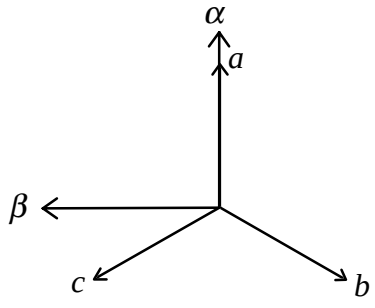


Figure 2.7 The superimposed three phase and two phase axes for the basic two pole motor.

Consider the transformation of the three phase stator currents, i_{1a}, i_{1b} and i_{1c} to the two phase stator currents, $i_{1\alpha}$ and $i_{1\beta}$. Resolving the components of the m.m.f. and thus the currents in the α and β directions:

$$\begin{aligned} i_{1\alpha} &= k(i_{1a} - i_{1b}\cos\pi/3 - i_{1c}\cos\pi/3) \\ &= k(i_{1a} - 0.5i_{1b} - 0.5i_{1c}) \end{aligned} \tag{2.23}$$

$$\begin{aligned} i_{1\beta} &= k(i_{1c}\sin\pi/3 - i_{1b}\sin\pi/3) \\ &= k(\frac{\sqrt{3}}{2}i_{1c} - \frac{\sqrt{3}}{2}i_{1b}) \end{aligned} \tag{2.24}$$

where *k* is a scale factor between the two systems. The value of *k* should be $\sqrt{2/3}$ for exact equivalence in power, but only proportional equivalence is required here so *k* can be any value.

There is no neutral connection, so:

$$i_{1a} + i_{1b} + i_{1c} = 0 \tag{2.25}$$

Using this in equation 2.23:

$$i_{1\alpha} = \frac{3}{2}ki_{1a} \tag{2.26}$$

Choose $k = 2/3$ to equalise $i_{1\alpha}$ and i_{1a}. Then the transform equations are:

$$i_{1\alpha} = i_{1a} \tag{2.27}$$

$$i_{1\beta} = \frac{1}{\sqrt{3}}(i_{1c} - i_{1b}) \tag{2.28}$$

For a balanced, symmetric machine, the same transform equations can be applied to the rotor voltages. The impedances transform unchanged. See O'Kelly and Simmons [2] for a more rigorous proof of these transforms. Using the transform equations, the equivalent circuit of Figure 2.5 transforms to that of Figure 2.8.

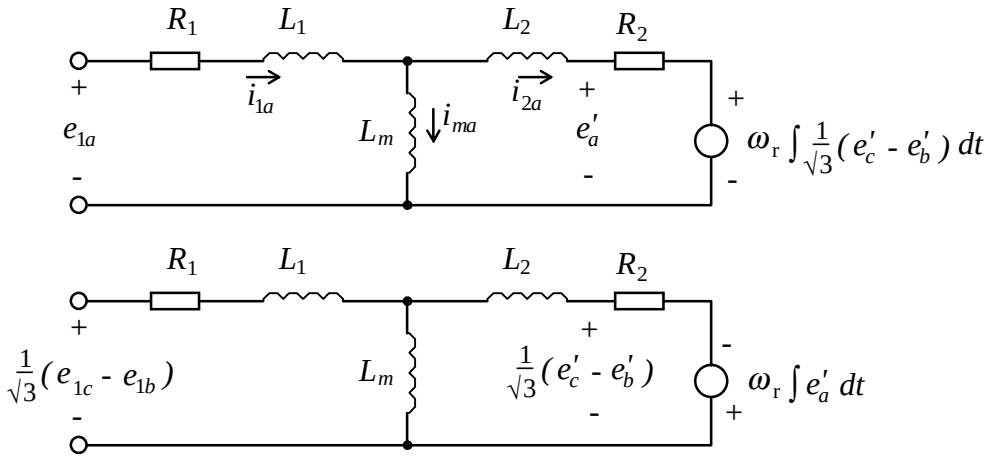


Figure 2.8 Two phase equivalent circuit with transformed variables. The α axis is aligned with the *a* phase.

Since the motor is symmetrical, the α axis could equally have been chosen to coincide with either the *b* or the *c* phase. If, for example, the α axis was aligned with the *b* phase, the two phase equivalent circuit would transform to that of Figure 2.9.

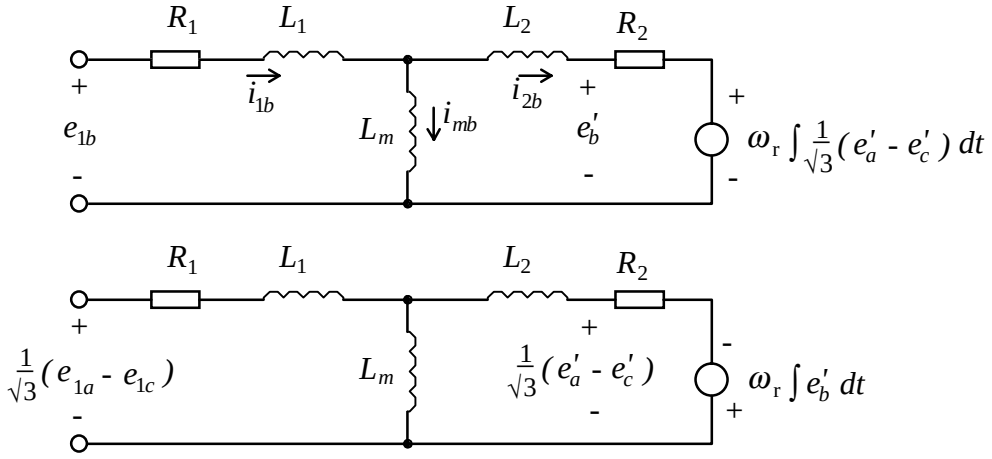


Figure 2.9 Two phase equivalent circuit with transformed variables. The α axis is aligned with the *b* phase.

The three alternate sets of circuits formed by different alignments of the α axis are all valid. Symmetry indicates the three sets of circuits can be combined into the one set of three circuits of Figure 2.10. These three circuits together form the three phase equivalent circuit of the induction motor.

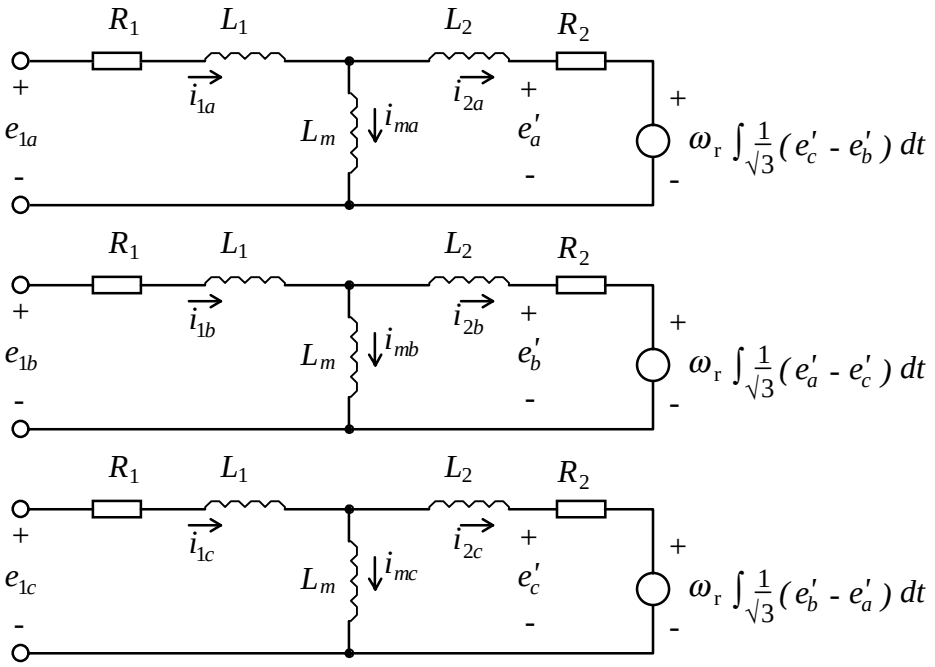


Figure 2.10 Three phase equivalent circuit.

The three phases of the equivalent circuit should always be connected in either star or delta configuration to ensure the requirement that $i_a + i_b + i_c = 0$ or $e_{1a} + e_{1b} + e_{1c} = 0$. Because of this requirement, the three phase equivalent circuit is not as intuitive as the two phase equivalent circuit of Figure 2.5 for understanding the operation of the induction motor, although it is a very useful equivalent circuit for use in circuit simulation packages such as Spice.

A check on the validity of the equivalent circuit of Figure 2.10 can be made using Kron's equations, equations 2.22. With the α axis aligned with the *a* phase, as in Figure 2.7, and with the rotor voltages set to zero, these equations transform into:

$$\begin{bmatrix} e_{1a} \\ \frac{1}{\sqrt{3}}(e_{1c} - e_{1b}) \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} R_1 + L_{11}p & 0 & L_m p & 0 \\ 0 & R_1 + L_{11}p & 0 & L_m p \\ L_m p & -\omega_r L_m & R_2 + L_{22}p & -\omega_r L_{22} \\ \omega_r L_m & L_m p & \omega_r L_{22} & R_2 + L_{22}p \end{bmatrix} \begin{bmatrix} i_{1a} \\ \frac{1}{\sqrt{3}}(i_{1c} - i_{1b}) \\ -i_{2a} \\ -\frac{1}{\sqrt{3}}(i_{2c} - i_{2b}) \end{bmatrix} \tag{2.29}$$

With the use of the relations $e_{1a}+e_{1b}+e_{1c}=0$, $i_{1a}+i_{1b}+i_{1c}=0$ and $i_{2a}+i_{2b}+i_{2c}=0$, equations 2.29 expand into the following set of six equations:

$$\begin{bmatrix} e_{1a} \\ e_{1b} \\ e_{1c} \\ 0 \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} R_1+L_{11}p & 0 & 0 & L_m p & 0 & 0 \\ 0 & R_1+L_{11}p & 0 & 0 & L_m p & 0 \\ 0 & 0 & R_1+L_{11}p & 0 & 0 & L_m p \\ L_m p & \omega_r L_m/\sqrt{3} & -\omega_r L_m/\sqrt{3} & R_2+L_{22}p & \omega_r L_{22}/\sqrt{3} & -\omega_r L_{22}/\sqrt{3} \\ -\omega_r L_m/\sqrt{3} & L_m p & \omega_r L_m/\sqrt{3} & -\omega_r L_{22}/\sqrt{3} & R_2+L_{22}p & \omega_r L_{22}/\sqrt{3} \\ \omega_r L_m/\sqrt{3} & -\omega_r L_m/\sqrt{3} & L_m p & \omega_r L_{22}/\sqrt{3} & -\omega_r L_{22}/\sqrt{3} & R_2+L_{22}p \end{bmatrix} \begin{bmatrix} i_{1a} \\ i_{1b} \\ i_{1c} \\ -i_{2a} \\ -i_{2b} \\ -i_{2c} \end{bmatrix}$$

(2.30)

These equations can also be obtained directly from the three phase equivalent circuit of Figure 2.10 by applying Kirchoff's laws to each of the six circuit loops, confirming the validity of the equivalent circuit.

2.3.7 Derivation of the Classical Steady State Equivalent Circuit

To check the validity of the above three phase equivalent circuit, it is used to derive the classical steady state per phase equivalent circuit for balanced three phase sinusoidal applied voltage waveforms.

For balanced sinusoidal waveforms, rotor voltages e'_a, e'_b, and e'_c are sinusoidal and displaced by $2\pi/3$ radians. For the *a* phase of the 3 phase equivalent circuit of Figure 2.10:

$$
\begin{aligned}
\text{let} \qquad & e'_a = V \sin \omega_o t \\
\text{then} \qquad & e'_b = V \sin\left(\omega_o t - \frac{2\pi}{3} \right) \\
& e'_c = V \sin\left(\omega_o t + \frac{2\pi}{3} \right) \\
& \frac{1}{\sqrt{3}}\left(e'_c - e'_b\right) = V \cos \omega_o t \\
\int \frac{1}{\sqrt{3}}\left(e'_c - e'_b\right) dt &= \frac{1}{\omega_o} V \sin \omega_o t \\
&= \frac{1}{\omega_o} e'_a
\end{aligned}
\tag{2.31}
$$

and the back e.m.f. voltage for phase *a* is $\frac{\omega_r}{\omega_o} e'_a$.

This back e.m.f. voltage and rotor resistance R_2 can be combined into a single resistance of value $R_2 \Big/ \left(1 - \frac{\omega_r}{\omega_o}\right) = R_2 / S$ where *S* is the rotor slip. This substitution in the phase *a* equivalent circuit in Figure 2.10 gives the classical equivalent circuit of Figure 2.11.

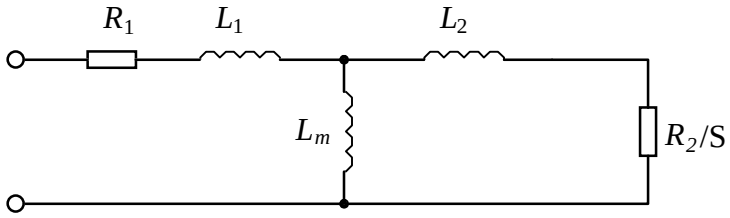


Figure 2.11 Classical steady state per phase equivalent circuit.

2.4 Power and Torque

From Figure 2.5, the mechanical power output, *P*, for a two phase motor is:

$$
P = \omega_r \left(i_{2\alpha} \int e'_\beta dt - i_{2\beta} \int e'_\alpha dt \right) \tag{2.32}
$$

For a motor with *n* pole pairs, the instantaneous torque is:

$$T = n\left(i_{2\alpha}\int e'_{\beta}dt - i_{2\beta}\int e'_{\alpha}dt\right) \tag{2.33}$$

Similar equations for the three phase motor can be derived from the equivalent circuit of Figure 2.10.

2.5 Some Observations from the Equivalent Circuit

The equivalent circuit of Figure 2.5 can be used to gain some intuitive insight into how the induction motor is affected by various applied voltages or currents.

First, it can be seen that the flux producing the motor back e.m.f., called the motor flux, has, as the quadrature components of its flux linkage, the integrals of the voltages e'_{α} and e'_{β}. The value of these voltages, in turn, depends partly on the back e.m.f.'s generated from these integrals, depending on the ratio of the total source impedance feeding the rotor circuit to the rotor resistance. This cross coupling forms a feedback oscillator the damping of which depends on the source impedance. The natural frequency of the oscillator is approximately the rotor frequency, ω_r, the exact value depending on the damping. For some values of capacitive source impedance, the damping will be negative resulting in self sustained oscillation. This effect is used in self excited induction generators.

Second, it can be seen that if the voltage drop across the leakage reactance and the stator resistance is neglected, the motor flux depends on the integral of the applied voltage. For minimum flux ripple, the ripple in this integral should be minimised. Also, to obtain the ideal sinusoidal motor flux waveform, it is more important to keep the integral of the applied voltage sinusoidal rather than the applied voltage itself.

3. THE NEW PHASE CONTROL METHOD - DOUBLE INTEGRAL CONTROL

3.1 Problems with Existing Phase Control Methods

In this section, the problems of existing phase control methods are examined using time domain methods rather than the traditional frequency domain analysis methods. It is found that the time domain analysis method gives a much deeper understanding of the cause of these problems.

3.1.1 Subharmonic Generation with Cosine Wave Crossing Control

Cosine wave crossing control was originally developed for DC thyristor drives and, provided there is no discontinuous current, produces an average DC output voltage which accurately reflects the DC reference voltage. When applied to a cycloconverter, though, where the reference voltage and the corresponding wanted average output voltage are rapidly varying, it is no longer accurate. This is illustrated in Figure 3.1, which shows three different reference waveforms of different average levels producing the same output waveform with cosine wave crossing control. The convex reference waveform of Figure 3.1(a) should result in a later trigger time and the concave waveform of Figure 3.1(c) should result in an earlier trigger time.

As can be seen from these examples, the reason why cosine wave crossing control produces the errors is that it determines the trigger angle from a sample of the reference waveform at one particular instance and ignores the shape of the reference waveform between these instances. These errors can build up over several input cycles resulting in DC or slowly varying AC offset errors in the average output voltage. This is the source of the output subharmonics which are the chief limiting factor in the upper frequency performance of a cycloconverter using cosine wave crossing control.

The above analysis is at odds with the analysis presented by Pelly [10]. In Chapter 11, page 290, Pelly states: ‘In Chapter 9 it is argued that the “cosine wave crossing” control method for determining the timing of the firing pulses is the “naturally correct” one for the cycloconverter, and this hypothesis is strengthened by the mathematical proof of the fact that this control method produces the theoretically minimum possible total r.m.s. distortion of the output waveform.’

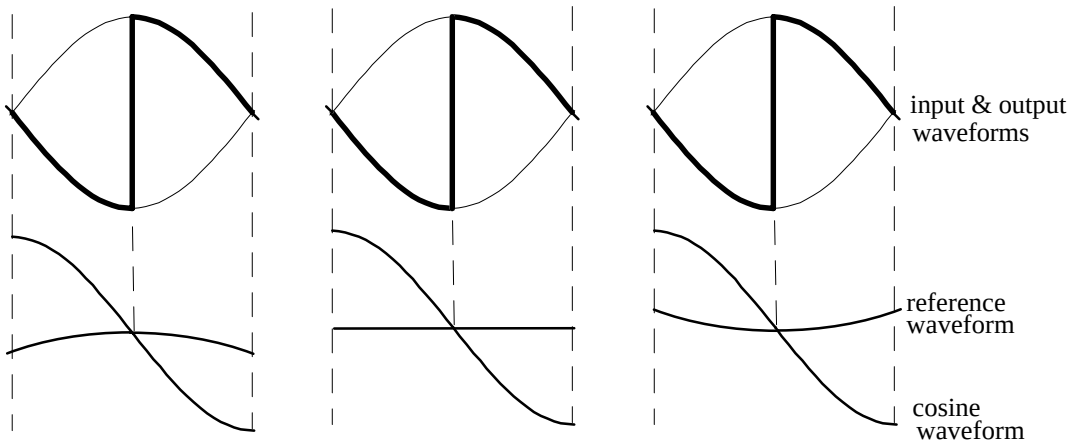


Figure 3.1. Examples of waveforms showing the inaccuracies of cosine wave crossing control. The different reference waveforms with different average levels produce the same output waveforms.

Pelly further states: '[the cosine wave crossing control method] has the unique property that it does not produce "unnecessary" direct integer multiple harmonics of the wanted output frequency.'

These points are often referred to in cycloconverter literature to defend the use of the cosine wave crossing control method. Neither point is correct. On the first point, the fact that cosine wave crossing control produces subharmonics means that it does not produce the minimum possible total harmonic distortion, for any subharmonic can be eliminated by adding to the reference waveform a subharmonic of equal amplitude but of opposite phase. This example also refutes the second point, since modifying the control method to eliminate a subharmonic in this way does not produce direct integer multiple harmonics of the wanted output frequency.

3.1.2 Distortion Problems with Integral Control and Pre-Integral Control

With the integral and pre-integral phase control methods (described in sections 1.4.3 and 1.4.4), output subharmonics cannot occur because the integral of the output is tightly controlled to match the integral of the reference at regular instances. On first inspection, it seems that integral control methods should be superior to cosine wave crossing control, but in practice this has not proved the case. It has been found [14] that integral control actually produces a much higher total harmonic distortion on the output with the

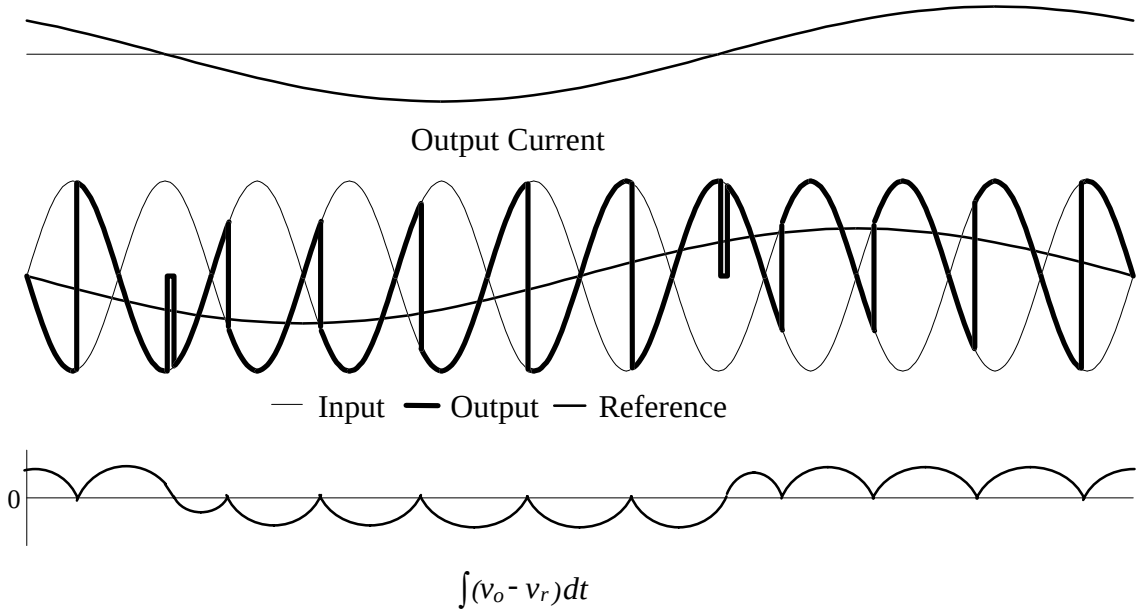


Figure 3.2 Illustration of distortion introduced with integral control

largest increase occurring in the low order direct harmonics of the wanted output frequency.

The reason for this increased distortion can be seen by examining the output waveforms in the time domain over a complete cycle of the output. This is shown in Figure 3.2 for integral control. The integral of the difference between the output and the reference voltages is approximately a square wave at the fundamental output frequency with superimposed ripple. It would have significant harmonics of the fundamental typical of a square wave. The presence of the square wave component is caused mainly by the integral having a DC offset of opposite polarity for the positive and negative banks.

3.2 Development of the Double Integral Control Algorithm

3.2.1 Definition of the operator $\int^{t_x}$

In the development of the double integral control algorithm, it will often be required to find the continuous integral of a variable in real time up to some fixed time, t_x. In a practical implementation, this integral is stored in computer memory and is initiated at the start of the computer program, usually to a value which will minimise any DC offset in the future calculated values of the integral. This integral is denoted by the new

operator $\int^{t_x}$ and will be used, for example, to represent the integral of v_o up to time t_1 with the term $\int^{t_1} v_o dt$.

3.2.2 Basic Double Integral Algorithm

As mentioned in section 2.5, to keep the motor flux sinusoidal with minimum flux ripple it is important to keep the integral of the applied voltage as close to sinusoidal as possible. A good phase control method for the cycloconverter should make this one of its chief aims. Cosine wave crossing control fails to meet this requirement because the voltage subharmonics generated in the output produce large deviations in the integral of its output voltage. Integral and pre-integral control fail because, as shown in section 3.1.2, they produce distorted voltage integral waveforms, although they do prevent subharmonic generation. The new phase control method described here, called double integral control, is developed directly from this basic requirement to keep the integral of the output voltage sinusoidal with minimum ripple thus ensuring that this condition is met.

To state the phase control problem more clearly, the requirement is to determine when to turn on each thyristor so that the integral of the output voltage is kept as close as possible to a reference voltage integral waveform which is normally sinusoidal. This pseudo flux is designated here as the integral of a reference voltage, $\int v_r dt$.

To simplify the problem, the output is first divided into time periods called trigger periods which are the same as those used for pre-integral control in section 1.4.4. The trigger periods are illustrated in Figure 3.3 for both 3-pulse and 2-pulse cycloconverters.

For a single phase input 2-pulse cycloconverter, the actual trigger period used in the experimental work in this thesis is the mains input half cycle. As shown in Figure 3.3, this differs from the ideal trigger period, but was found in practice to be close enough to not affect performance. The advantage of having a trigger period which is synchronised to the mains is that it greatly reduces the calculations required to determine the triac trigger instant.

As stated above, the requirement in choosing the trigger instant is to keep the integral of the output voltage as close as possible to a reference voltage integral. This can be done

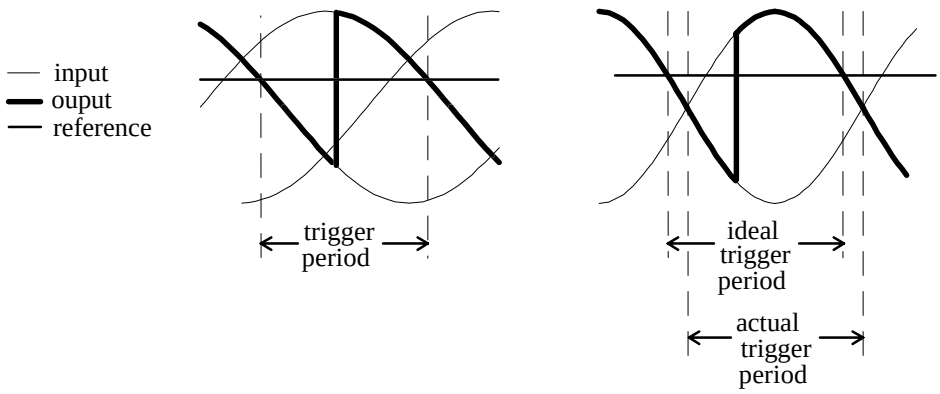


Figure 3.3 Trigger periods for 3-pulse and 2-pulse cycloconverters used for double integral control.

over the time of one trigger period by choosing the trigger instant so that the average over a trigger period of the difference between the reference voltage integral and the integral of the output voltage is zero. This is expressed in the following relation:

$$0 = \int_{t_1}^{t_2} \left(\int^{t} v_o dt - \int^{t} v_r dt \right) dt \tag{3.1}$$

Where t_1 and t_2 are the start and end times of the trigger period.

3.2.3 Correction for Instability

The above algorithm fulfils the requirements but unfortunately can result in unstable operation if implemented in practice. An example of this instability is shown in Figure 3.4 for a 2-pulse cycloconverter. It is similar to the instability shown in Figure 1.12 for integral control. For a practical implementation of this algorithm, some method must be devised to suppress the instability.

Observation of the integral of the error voltage in Figure 3.4 shows that the difference in its values at the start and end of each trigger period is large when the output is unstable, but would be close to zero for a stable output. This difference can be used to stabilise the output by adding a proportion of it to the R.H.S of equation 3.1 in the right sense to suppress the instability. This modification is shown in equation 3.2. The constant K sets the proportion. It is multiplied by $(t_2 - t_1)$ to make it dimensionless.

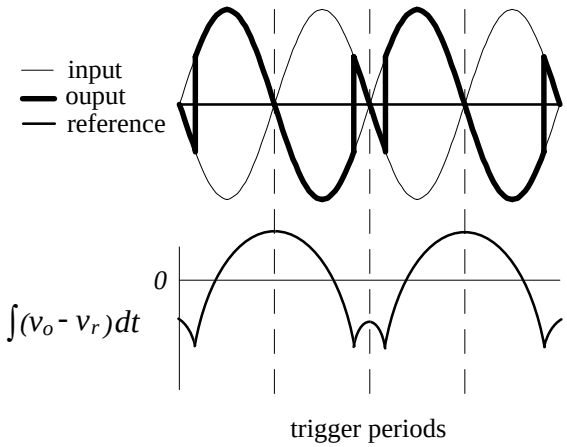


Figure 3.4 An example of instability in a 2-pulse cycloconverter that can occur for double integral control with no stabilising terms.

$$0 = \int_{t_1}^{t_2} \int^{t} (v_o - v_r)dt^2 + K(t_2 - t_1)\int_{t_1}^{t_2} (v_o - v_r)dt \tag{3.2}$$

To estimate the value of *K*, a simulation of the output for the simple case of a 2-pulse cycloconverter with zero reference voltage and continuous operation in the positive bank is conducted. The simulation uses the normalised trigger period shown in Figure 3.5. The reference voltage is set to 0 and the input voltage waveform has an amplitude of one and a period of 2π. The thyristor trigger time is denoted by t_f.

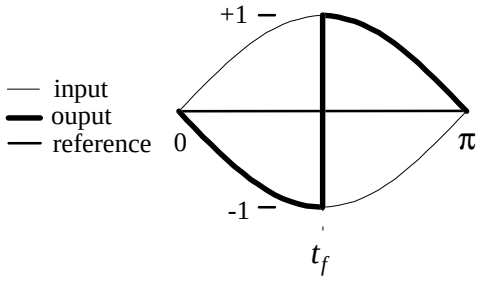


Figure 3.5 Normalised trigger period for the simulation used to determine the constant *K* for a 2-pulse cycloconverter.

For this trigger period, equation 3.2 becomes:

$$0 = \int_0^{\pi} \int^{t} v_o dt^2 + K\pi \int_0^{\pi} v_o dt \tag{3.3}$$

Setting the output voltage to $-\sin t$ up to time t_f and $\sin t$ from time t_f, equation 3.3 expands to: (see Appendix A)

$$0 = \pi \int_0^0 v_o dt + 2\sin t_f + 2(K\pi + \pi - t_f)\cos t_f - \pi \tag{3.4}$$

Also, the value of the integral of v_o at the end of the period is given by the equation: (see Appendix A for the derivation)

$$\int_\pi^\pi v_o dt = \int_0^0 v_0 dt + 2\cos t_f \tag{3.5}$$

The simulation was undertaken for 5 trigger periods. Equation 3.4 was solved for t_f consecutively for each period with the integral of v_o at the start of the period set to its value at the end of the previous period, which is found using equation 3.5. For the first period, this integral was initially set to zero. The simulation was repeated for various values of *K* with the values of the integral of v_o at the start of each period recorded. A spreadsheet was used for the simulation. The results are shown in Table 3.1.

Table 3.1 Variation of the integral of v_o at the start of consecutive trigger periods with different values of *K* from a simulation of a 2-pulse cycloconverter.

K	Integral of v_o at start of period No.:					
	1	2	3	4	5	6
0.3	0	0.4353	0.3446	0.3680	0.3622	0.3637
0.4	0	0.3902	0.3603	0.3637	0.3633	0.3634
0.5	0	0.3534	0.3634	0.3634	0.3634	0.3634
0.6	0	0.3228	0.3596	0.3630	0.3633	0.3634
0.7	0	0.2970	0.3521	0.3615	0.3631	0.3633

It can be seen from this table that the optimum value of *K* for fastest convergence is approximately 0.5. Lower values result in underdamped response and higher values result in overdamped response. Note the fast recovery after a disturbance with *K* set to

0.5. The integral of v_o recovers to 97% of its steady state value in the first trigger period after the disturbance.

This simulation is for the ideal case where the current is continuous. For the case where the current is discontinuous, a simulation using the waveforms of Figure 3.6 was undertaken. This is an extreme case of discontinuous current where the thyristor turns off at the start of the period and the output voltage reverts to a normalised value of -0.3 representing a possible motor back e.m.f.

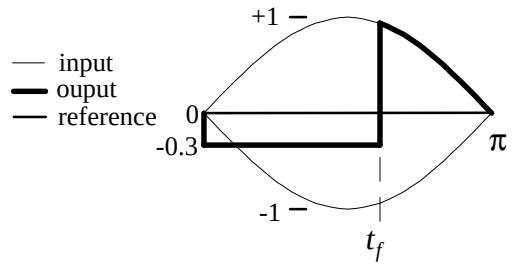


Figure 3.6 Waveforms used for the simulation for determining the stability constant, *K*, for the case of discontinuous current.

For the simulated trigger period, equation 3.2, using the same expansion method as in Appendix A, expands to the equation:

$$0 = \pi\int^{0} v_o dt - 0.15{t_f}^2 + \left(K\pi + \pi - t_f\right)\left(\cos t_f - 0.3t_f\right) + \sin t_f + K\pi \qquad (3.6)$$

Also, the value of the integral of v_o at the end of the period is given by the equation:

$$\int^{\pi} v_o dt = \int^{0} v_o dt - 0.3t_f + 1 + \cos\left(t_f\right) \qquad (3.7)$$

The result of the simulation is shown in table 3.2.

In this simulation, the optimum value of *K* is about 0.6, not 0.5 as before. Ideally, *K* should be varied according to the situation, but in the experimental work done for this thesis, *K* was kept at 0.5. The above simulation shows that the error introduced with this approximation is not large.

Table 3.2 Variation of the integral of v_o at the start of consecutive trigger periods with different values of *K* from a simulation of a 2-pulse cycloconverter with discontinuous current.

K	Integral of v_o at start of period No.:					
	1	2	3	4	5	6
0.3	0	0.3705	0.2070	0.2923	0.2509	0.2718
0.4	0	0.3272	0.2449	0.2708	0.2631	0.2654
0.5	0	0.2927	0.2605	0.2656	0.2648	0.2649
0.6	0	0.2645	0.2649	0.2649	0.2649	0.2649
0.7	0	0.2411	0.2633	0.2648	0.2649	0.2649

3.2.4 Alternative Derivation: Minimising Ripple Current

The double integral algorithm was developed in the previous section from the requirement that the integral of the output voltage be kept as close as possible to a reference voltage integral waveform which is normally sinusoidal. Another desirable property for a phase control algorithm is to minimise the ripple current of the motor. It will be shown in this section that this requirement is also met with the double integral control algorithm.

At the ripple current frequencies, the motor impedance is dominated by its leakage reactance and the motor per phase equivalent circuit can be approximated by that of Figure 3.7. The voltage developed across the motor resistance plus the motor back e.m.f. has negligible ripple component compared to the ripple voltage across the motor leakage inductance, *L*, and so would be approximately the same as the cycloconverter reference voltage, v_r, making the voltage across the motor leakage inductance, *L*, the same as the difference between the cycloconverter output and reference voltages. The ripple current in the motor, i_{ripple}, is thus given approximately by:

$$i_{ripple} = \frac{1}{L}\int (v_o - v_r)dt \qquad (3.8)$$

The ripple current can be minimised by making the average of the ripple current over each trigger period equal to zero. This results in the basic double integral algorithm of equation 3.1. Thus minimum ripple current and minimum flux error are both produced by the double integral control algorithm.

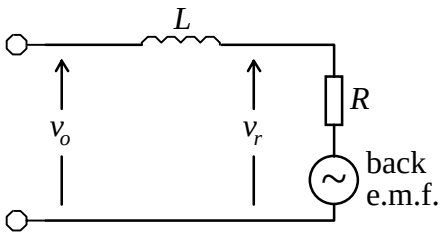


Figure 3.7 Per phase high frequency equivalent circuit of an induction motor with values of the cycloconverter output and reference voltages shown.

3.3 Practical implementation

3.3.1 Implementation of the Double Integral Algorithm

Before developing a practical implementation of the algorithm of equation 3.2, some important properties of the cycloconverter output waveform need to be considered. First, from the time a thyristor is triggered to the end of the trigger period, the output current will never be zero because the output voltage will always be greater than the reference voltage causing the thyristor current to increase. During this part of the trigger period, the output voltage will be equal to the mains input voltage and so can be accurately determined in advance. Second, from the start of the trigger period to the time the thyristor is triggered, the opposite effects occur and the current is always falling. During this period, the thyristor current can drop to zero, turning the thyristor off. The motor voltage then depends on the motor back e.m.f. and the coupling from the other motor phases and so cannot be determined in advance.

A practical method of implementing the double integral algorithm which takes these properties into consideration is as follows: The trigger period is divided into sampling intervals of fixed time width, the time width of these intervals being determined by the trigger phase error that can be tolerated. Generally intervals of less than 300 microseconds are required. At each sampling interval, the R.H.S. of equation 3.2 is evaluated for the case where the thyristor is triggered at this sampling interval. When the sample interval is reached where the value of this expression has reached zero or changed sign, the thyristor is triggered.

The evaluation of the R.H.S. of equation 3.2 is difficult and must be done in a short time. It has been found in practice that a high speed digital signal processor is required.

To evaluate the expression, the continuous integral of the output voltage must first be measured. This measurement must have high long term accuracy to avoid DC offset errors in the output voltage. The easiest way to achieve this is with an integrating type voltage to frequency converter, which has high integrating accuracy and a pulse output which can be easily electrically isolated. The output pulses go to a counter, the value of which is the continuous integral of the output voltage. One problem is that the voltage to frequency converter has a unipolar input whereas a bipolar input is required. This is overcome by adding a fixed DC offset to the input of the converter and a corresponding continuous down count to the counter.

The next step is to expand the R.H.S. of equation 3.2 into a form which can be computed by the digital signal processor. The expression needs to be expanded to maximise the number of calculations that need only be done once for a trigger period instead of every sample time and to use look-up tables wherever possible.

Let v_t be the mains input voltage which is connected to the output after the thyristor in the current trigger period is turned on. Assume initially the output operates at a fixed voltage to frequency ratio without voltage boost at lower frequencies, allowing $\int^t v_r dt$ to be replaced by a predetermined voltage integral waveform, $\psi(t)$, which can be stored in a look-up table. The expansion is developed as follows:

$$
\begin{aligned}
&\int_{t_1}^{t_2}\int^{t}(v_o - v_r)dt^2 + K(t_2 - t_1)\int_{t_1}^{t_2}(v_o - v_r)dt \\
&= \int_{t_1}^{t_f}\int^{t} v_o dt^2 + \int_{t_f}^{t_2}\int^{t} v_o dt^2 - \int_{t_1}^{t_2}\int^{t} v_r dt^2 \\
&\quad + K(t_2 - t_1)\left\{\int^{t_f} v_o dt - \int^{t_1} v_o dt + \int_{t_f}^{t_2} v_o dt - \int_{t_1}^{t_2} v_r dt\right\} \\
&= \int_{t_1}^{t_f}\int^{t} v_o dt^2 + \int_{t_f}^{t_2}\int^{t} v_o dt^2 - \int_{t_1}^{t_2} \psi(t) dt \\
&\quad + K(t_2 - t_1)\left\{\int^{t_f} v_o dt - \int^{t_1} v_o dt + \int_{t_f}^{t_2} v_t dt - \psi(t_2) + \psi(t_1)\right\}
\end{aligned}
$$

(3.9)

The term $\int_{t_f}^{t_2}\int^{t} v_o dt^2$ expands as follows:

$$\begin{aligned}\int_{t_f}^{t_2}\int^{t} v_o dt^2 &= \int_{t_f}^{t_2}\int^{t_f} v_o dt^2 + \int_{t_f}^{t_2}\int_{t_f}^{t} v_o dt^2 \\ &= \left(t_2 - t_f\right)\int^{t_f} v_o dt + \int_{t_f}^{t_2}\int_{t_f}^{t} v_t dt^2\end{aligned} \tag{3.10}$$

The term $\int_{t_f}^{t_2}\int_{t_f}^{t} v_t dt^2$ must be computed for each sample time but this is a very long calculation. This term can be more easily computed by making use of the following relation:

$$\begin{aligned}\int_{t_0}^{t_2}\int_{t_0}^{t} v_t dt^2 &= \int_{t_0}^{t_f}\int_{t_0}^{t} v_t dt^2 + \int_{t_f}^{t_2}\int_{t_0}^{t} v_t dt^2 \\ &= \int_{t_0}^{t_f}\int_{t_0}^{t} v_t dt^2 + \left(t_2 - t_f\right)\int_{t_0}^{t_f} v_t dt + \int_{t_f}^{t_2}\int_{t_f}^{t} v_t dt^2\end{aligned} \tag{3.11}$$

Where t_0 can be any arbitrary time, but for this case is chosen to be a time fixed in phase to the input waveform to allow table look-up evaluation of the integrals.

Thus, $\int_{t_f}^{t_2}\int_{t_f}^{t} v_t dt^2$ expands to:

$$\int_{t_f}^{t_2}\int_{t_f}^{t} v_t dt^2 = \int_{t_0}^{t_2}\int_{t_0}^{t} v_t dt^2 - \int_{t_0}^{t_f}\int_{t_0}^{t} v_t dt^2 - \left(t_2 - t_f\right)\int_{t_0}^{t_f} v_t dt \tag{3.12}$$

The three integrals in the expansion can be easily computed using look-up tables (two tables would be required, one for the double integrals and one for the single integral). Also, the first term need only be computed once for each trigger period.

Also, the term $\int_{t_f}^{t_2} v_t dt$ in equation 3.9 expands to:

$$\int_{t_f}^{t_2} v_t dt = \int_{t_0}^{t_2} v_t dt - \int_{t_0}^{t_f} v_t dt \tag{3.13}$$

The terms in this expansion can be conveniently computed from the same single integral look-up table.

Rewriting and rearranging equation 3.9 with the above expansions included:

$$
\begin{aligned}
0 = & \int_{t_0}^{t_2}\int_{t_0}^{t} v_t dt^2 + K(t_2 - t_1)\int_{t_0}^{t_2} v_t dt \\
& - \int_{t_1}^{t_2} \psi(t) dt - K(t_2 - t_1)\left[\psi(t_2) - \psi(t_1)\right] \\
& - K(t_2 - t_1)\int^{t_1} v_o dt \\
& + \int_{t_1}^{t_f}\int^{t} v_o dt^2 + (t_2 - t_f)\int^{t_f} v_o dt + K(t_2 - t_1)\int^{t_f} v_o dt \\
& - \int_{t_0}^{t_f}\int_{t_0}^{t} v_t dt^2 - (t_2 - t_f)\int_{t_0}^{t_f} v_t dt - K(t_2 - t_1)\int_{t_0}^{t_f} v_t dt
\end{aligned}
\qquad (3.14)
$$

The R.H.S. of this equation needs to be evaluated every sample time, but the terms in the first three lines need to be computed only once at the start of each trigger period. For the remaining terms, the integrals involving v_t can be found from look-up tables, the integral of v_o can be read from the V/f converter and the double integral of v_o can be easily calculated numerically using a step size of one sample interval.

For the experimental three phase cycloconverter described in chapter 5, the readings from the flux look-up table are multiplied by a variable in real time to allow for operation with variable motor flux. Also, readings from the look-up table involving the input voltage are multiplied by a variable to allow for adjustments to variations in input voltage. For the experimental work described in this thesis, both these variables are fixed, with all tests conducted with fixed values of flux and input voltage.

3.3.2 Adding Voltage Boost

As the speed of an induction motor is reduced by reducing the applied frequency and voltage, the stator IR drop becomes a significant proportion of the motor voltage and must be compensated for by adding a boost voltage. This is not easy to implement using the algorithm of equation 3.14, where the reference flux $\psi(t)$ would have to increase towards infinity as the output frequency is reduced to zero.

To implement voltage boost, equation 3.14 has to be modified. To see how this can be done, replace v_r in equation 3.2 (which is the contracted form of equation 3.14) with $v_\psi + v_b$, where v_ψ is the component of the reference voltage which is proportional to the frequency and v_b is the boost component, and rearrange as follows:

$$\begin{aligned} 0 &= \int_{t_1}^{t_2}\int^{t}(v_o - v_r)dt^2 + K(t_2 - t_1)\int_{t_1}^{t_2}(v_o - v_r)dt \\ &= \int_{t_1}^{t_2}\int^{t}(v_o - v_b - v_\psi)dt^2 + K(t_2 - t_1)\int_{t_1}^{t_2}(v_o - v_b - v_\psi)dt \end{aligned} \tag{3.15}$$

This equation indicates that voltage boost can be incorporated by expanding equation 3.2 as in section 3.3.1 above but with v_o replaced by $v_o - v_b$. This should remove from the expansion integral terms which go to infinity as the frequency goes to zero. With this substitution, v_o in equation 3.14 must be replaced with $v_o - v_b$ and v_t with $v_t - v_b$. The terms in v_t in equation 3.14 then become:

$$\begin{aligned} &\int_{t_0}^{t_2}\int_{t_0}^{t}(v_t - v_b)dt^2 + K(t_2 - t_1)\int_{t_0}^{t_2}(v_t - v_b)dt \\ &-\int_{t_0}^{t_f}\int_{t_0}^{t}(v_t - v_b)dt^2 - (t_2 - t_f)\int_{t_0}^{t_f}(v_t - v_b)dt - K(t_2 - t_1)\int_{t_0}^{t_f}(v_t - v_b)dt \\ &= \int_{t_0}^{t_2}\int_{t_0}^{t}v_t dt^2 + K(t_2 - t_1)\int_{t_0}^{t_2}v_t dt \\ &-\int_{t_0}^{t_f}\int_{t_0}^{t}v_t dt^2 - (t_2 - t_f)\int_{t_0}^{t_f}v_t dt - K(t_2 - t_1)\int_{t_0}^{t_f}v_t dt \\ &-\int_{t_0}^{t_2}\int_{t_0}^{t}v_b dt^2 - K(t_2 - t_1)\int_{t_0}^{t_2}v_b dt \\ &+\int_{t_0}^{t_f}\int_{t_0}^{t}v_b dt^2 + (t_2 - t_f)\int_{t_0}^{t_f}v_b dt + K(t_2 - t_1)\int_{t_0}^{t_f}v_b dt \end{aligned} \tag{3.16}$$

It was shown in section 3.3.1 that t_0 can be set to any arbitrary value for the terms in v_t. This also applies to the terms in v_b in the R.H.S. of equation 3.16 above since they have the same form. The boost integral terms cannot be found using look-up tables. They must be evaluated numerically, so choose t_0 for these terms to be the start of the trigger period, t_1.

With the above modifications, equation 3.14 becomes:

$$
\begin{aligned}
0 = & \int_{t_0}^{t_2}\int_{t_0}^{t} v_t dt^2 + K(t_2 - t_1)\int_{t_0}^{t_2} v_t dt \\
& - \int_{t_1}^{t_2}\int_{t_1}^{t} v_b dt^2 - K(t_2 - t_1)\int_{t_1}^{t_2} v_b dt \\
& - \int_{t_1}^{t_2} \psi(t) dt - K(t_2 - t_1)\left[\psi(t_2) - \psi(t_1)\right] \\
& - K(t_2 - t_1)\int^{t_1} (v_o - v_b) dt \\
& + \int_{t_1}^{t_f}\int^{t} (v_o - v_b) dt^2 + (t_2 - t_f)\int^{t_f} (v_o - v_b) dt + K(t_2 - t_1)\int^{t_f} (v_o - v_b) dt \\
& - \int_{t_0}^{t_f}\int_{t_0}^{t} v_t dt^2 - (t_2 - t_f)\int_{t_0}^{t_f} v_t dt - K(t_2 - t_1)\int_{t_0}^{t_f} v_t dt \\
& + \int_{t_1}^{t_f}\int_{t_1}^{t} v_b dt^2 + (t_2 - t_f)\int_{t_1}^{t_f} v_b dt + K(t_2 - t_1)\int_{t_1}^{t_f} v_b dt
\end{aligned}
$$

(3.17)

This algorithm can be implemented as before, except for some differences due to the terms added or modified from the addition of voltage boost. First, the integral of $(v_o - v_b)$ can be derived simply by incrementing or decrementing the V/f counter by an amount corresponding to the instantaneous reference value of the voltage boost (which can be found from a look-up table) at each sample time so that the counter value corresponds to the required integral. Second, the integrals and double integrals of v_b must be found by numerical integration, using a look-up table to find the instantaneous values of v_b.

The above method of adding voltage boost is quite accurate and allows the voltage boost to be modified rapidly on demand, as required to implement vector control of the induction motor, but it suffers from needing excessive computation time. The method is used for the experimental 3 phase cycloconverter described later. This dynamic accuracy is not required for low cost cycloconverter drives without vector control such as the single phase input cycloconverter drive which will also be described later. For this type of drive, the algorithm of equation 3.17 can be simplified.

For drives without vector control, the amplitude of voltage boost does not change rapidly and boost need only be applied at low speed. In this case, by assuming that the integral of voltage boost does not change for the duration of one trigger period, the practical implementation of voltage boost can be greatly simplified. To do this, expand equation 3.15 as follows:

$$
\begin{aligned}
0 &= \int_{t_1}^{t_2}\int^{t}\left(v_o - v_b - v_\psi\right)dt^2 + K\left(t_2 - t_1\right)\int_{t_1}^{t_2}\left(v_o - v_b - v_\psi\right)dt \\
&= \int_{t_1}^{t_2}\int^{t_1}\left(v_o - v_b\right)dt^2 + \int_{t_1}^{t_2}\int_{t_1}^{t} v_o dt^2 - \int_{t_1}^{t_2}\int_{t_1}^{t} v_b dt^2 - \int_{t_1}^{t_2}\int^{t} v_\psi dt^2 \\
&\quad + K\left(t_2 - t_1\right)\left[\int_{t_1}^{t_2}\left(v_o - v_\psi\right)dt - \int_{t_1}^{t_2} v_b dt\right]
\end{aligned}
\tag{3.18}
$$

If it is assumed that the integral of voltage boost does not change over the trigger period then the terms $\int_{t_1}^{t_2}\int_{t_1}^{t} v_b dt^2$ and $\int_{t_1}^{t_2} v_b dt$ are zero. Also, define a new variable, v_o', as follows:

$$
\begin{aligned}
v_o' &= v_o - v_b \quad \text{for} \quad t < t_1 \\
v_o' &= v_o \qquad\quad \text{for} \quad t \geq t_1
\end{aligned}
\tag{3.19}
$$

With these substitutions, equation 3.18 reduces to:

$$
0 = \int_{t_1}^{t_2}\int^{t}\left(v_o' - v_\psi\right)dt^2 + K\left(t_2 - t_1\right)\int_{t_1}^{t_2}\left(v_o' - v_\psi\right)dt \tag{3.20}
$$

This equation is of the same form as equation 3.2 and expands similarly to the same form as equation 3.14, giving the equation:

$$
\begin{aligned}
0 &= \int_{t_0}^{t_2}\int_{t_0}^{t} v_t dt^2 + K\left(t_2 - t_1\right)\int_{t_0}^{t_2} v_t dt \\
&\quad - \int_{t_1}^{t_2}\psi(t)dt - K\left(t_2 - t_1\right)\left[\psi\left(t_2\right) - \psi\left(t_1\right)\right] \\
&\quad - K\left(t_2 - t_1\right)\int^{t_1} v_o' dt \\
&\quad + \int_{t_1}^{t_f}\int^{t} v_o' dt^2 + \left(t_2 - t_f\right)\int^{t_f} v_o' dt + K\left(t_2 - t_1\right)\int^{t_f} v_o' dt \\
&\quad - \int_{t_0}^{t_f}\int_{t_0}^{t} v_t dt^2 - \left(t_2 - t_f\right)\int_{t_0}^{t_f} v_t dt - K\left(t_2 - t_1\right)\int_{t_0}^{t_f} v_t dt
\end{aligned}
\tag{3.21}
$$

To implement this algorithm, the integral of v_o' can be found for each trigger period by the following process: During each trigger period, the integral of the boost voltage from time t_1 is calculated numerically by adding the table look-up values of the boost voltage at each sample time. This total is then subtracted from the v/f counter value at the start of the next trigger period. This counter value will then always be the integral of v_o'. With this change, the algorithm can be implemented in the same way as equation 3.14.

3.3.3 Simplification for 2-pulse Cycloconverters

For the case of the single phase, 2-pulse cycloconverter, where the approximate trigger period shown in Figure 3.3 is used, further reductions in the algorithm computations can be made. From equations 3.9 and 3.10, the unexpanded terms in v_t in the double integral algorithms are:

$$\int_{t_f}^{t_2}\int_{t_f}^{t} v_t dt^2 + K(t_2 - t_1)\int_{t_f}^{t_2} v_t dt \tag{3.22}$$

Since time t_2 is fixed in phase to the input waveform, v_t, and the interval $(t_2 - t_1)$ is the same for every trigger period (assuming a fixed mains frequency), the above expression has only one variable, t_f, and can be found using one look-up table. Using this expression for the v_t terms, the algorithm of equation 3.21 can be reduced to:

$$\begin{aligned} 0 = &-\int_{t_1}^{t_2} \psi(t)dt - K(t_2 - t_1)\left[\psi(t_2) - \psi(t_1)\right] \\ &-K(t_2 - t_1)\int^{t_1} v_o' dt \\ &+\int_{t_1}^{t_f}\int^{t} v_o' dt^2 + (t_2 - t_f)\int^{t_f} v_o' dt + K(t_2 - t_1)\int^{t_f} v_o' dt \\ &+\int_{t_f}^{t_2}\int_{t_f}^{t} v_t dt^2 + K(t_2 - t_1)\int_{t_f}^{t_2} v_t dt \end{aligned} \tag{3.23}$$

This is the form of the double integral algorithm used in the low cost 2-pulse cycloconverter described later.

3.3.4 Additions for Vector Control

The double integral control method can be incorporated into a vector control scheme if the boost voltage can be modified rapidly, such as can be achieved if equation 3.17 is used for the control algorithm. The flux reference waveform, $\psi(t)$, can be used to match the actual motor flux, and the amplitudes of the in phase and quadrature components of the boost voltage, v_t, can be used in the current feedback loop to control the motor current.

3.3.5 Varying Frequency and Boost

There is a problem in rapidly varying the output frequency or the boost amplitude or phase because the double integral control method requires a knowledge of the output waveform in advance from the time a thyristor is triggered to the end of the trigger period. Further, if the expansions of the double integral control algorithm described above are used, where some of the calculations are done once at the start of the trigger period, this knowledge is required from the start of the trigger period. This problem is solved by inserting a suitable software delay between the time the frequency and boost variables are sampled to the time they are used. This allows these variables to be known in advance, although at the cost of a reduction in system response time. This delay can be minimised by recalculating the whole double integral algorithm at every sample time rather than splitting off the most computationally intensive sections to be calculated only once at the start of each trigger period. This has not been attempted in this thesis.

3.4 Bank Cross-Over Technique

As explained in section 1.5, a major problem with cycloconverters using existing phase control techniques is the selection of the time when to change banks. The techniques in common use are either to look for the first current zero, which requires the output current of the cycloconverter to be mostly free of discontinuous current, or, in current feedback systems, to use the zero crossing of the current reference. These systems, however, require a cycloconverter of high pulse number for stability. With 2-pulse cycloconverters, neither method can work.

With double integral control, these problems disappear. The bank cross-over selection time can be determined accurately and simply even for 2-pulse cycloconverters with discontinuous current occurring during every trigger period. The method is as follows.

It was shown in section 3.2.4 that the motor ripple current is approximately proportional to the integral of the difference between the output and reference voltages. This was expressed in equation 3.8. The value of this integral is readily available from the double integral control algorithm. Its polarity is the polarity of the ripple component of the output current.

The bank cross-over time is chosen to be the first time when the actual current is zero (and thus all thyristors in that phase are off) and the polarity of the integral of $v_o - v_r$, is positive for the positive bank, or negative for the negative bank. This corresponds to the first time the current is zero after the fundamental component of the current has passed through zero, which is probably the optimum bank cross-over time. This is illustrated in Figure 8 for the positive bank. Zero current is determined by monitoring the voltages across the thyristors. When the voltages across the thyristors in the phase are all greater than the thyristor maximum on voltage, the current in that phase must be zero. This method was first developed by Hamblin and Barton [18].

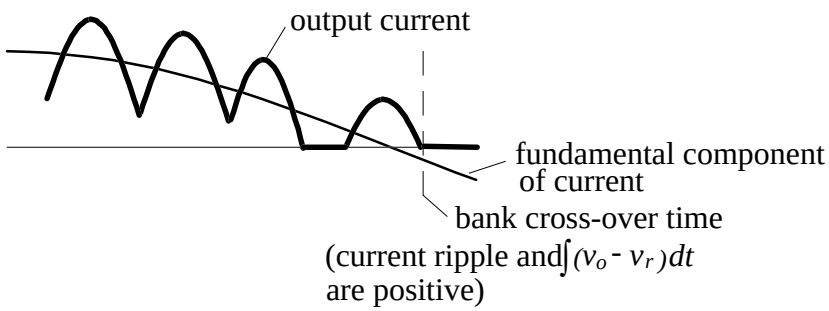


Figure 3.8 Illustration of bank cross-over selection time for the positive bank. Output current must be zero and the integral of $v_o - v_r$ must be positive.

When the cycloconverter has a 3 phase load with no neutral connection, such as a 3 phase induction motor, an extra modification must be made to compensate for the absence of zero sequence components of current on the outputs. Any voltage distortion that is common to all three outputs does not produce any corresponding current ripple. The instantaneous value of the current ripple in a particular output is in this case proportional to the integral of $v_o - v_r$ less the common mode component. This is expressed as follows:

$$\text{ripple current} \propto \int (v_o - v_r)dt - \frac{1}{3}\sum_{U,V,W}\int (v_o - v_r)dt \qquad (3.24)$$

To compensate for this, the bank cross-over time is now chosen to be the first instant when the output current is zero and the expression on the right hand side of equation 3.24 is positive for the positive bank and negative for the negative bank.

A problem with the double integral control technique is how to resume normal operation after a change in banks. One method is to select the first trigger period after the bank change to extend back to the start of the last trigger period of the previous bank and to end at the next normal trigger period end point. With this method, a correction to the stabilising term of equation 3.2 is required because with the integral of $v_o - v_r$ being positive at the end of a trigger period for the positive bank but negative at the end of a trigger period for the negative bank, the stabilising term for the trigger period encompassing the bank cross-over time will have a large, unwanted value. The solution, for this trigger period only, is to use equation 3.25 below instead of equation 3.2 for the double integral algorithm.

$$0 = \int_{t_1}^{t_2} \int^{t} (v_o - v_r) dt^2 + K(t_2 - t_1)\left(-\int^{t_1} (v_o - v_r) dt - \int^{t_2} (v_o - v_r) dt \right) \qquad (3.25)$$

In this new equation, the sign of the initial value of the integral in the stability term is reversed.

This method is used in the experimental 2-pulse, single phase to two phase cycloconverter. The method was also tried in the experimental 3-pulse cycloconverter but difficulties were encountered. It was found that an abnormally high current pulse occurred in the output current waveform, probably because of the extended trigger period that can occur during the bank cross-over as shown in Figure 3.9. Instead, a different method using a trial and error approach was used.

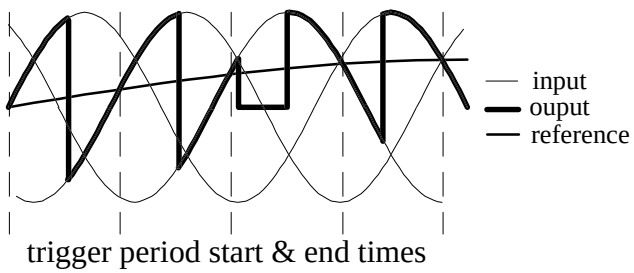


Figure 3.9 An example of bank cross-over from the negative to the positive bank for a 3-pulse cycloconverter showing the extended time between the start and end of trigger periods.

In this alternative method, the first trigger period after the bank change over starts at the bank change over time. The algorithm used for this trigger period is that of the equation:

$$0 = \int_{t_1}^{t_2} \int^{t} (v_o - v_r) dt^2 + K(t_2 - t_1)\left(A - \int^{t_2} (v_o - v_r) dt \right) \tag{3.26}$$

where the constant, *A*, is set to minimise current ripple during cross-over. This constant should be set to the expected value of the voltage integral $\int (v_o - v_r) dt$ at the start of the trigger period immediately following the bank change assuming no instability. This will force this integral to stabilise at its steady state value as quickly as possible after the bank change. This method seems to work well in practice but it is not ideal. It ignores the shape of the integral of v_o waveform before the bank change-over time. More research is required to find a better alternative.

4. THE SPLIT PHASE TRIAC CYCLOCONVERTER DRIVING A 2-PHASE INDUCTION MOTOR

The first of the two experimental cycloconverters developed using the double integral control technique is a single phase to two phase, 2-pulse cycloconverter designed to drive a specially wound two phase induction motor with a centre tapped winding on each phase. It was developed with low cost being the most important parameter.

4.1 Power Circuit

Each motor phase is controlled by a one phase, 2-pulse cycloconverter consisting of two triacs. Figure 4.1 shows the complete power circuit for one phase. The circuit of the other phase is identical. The circuit is exactly equivalent in operation to the more familiar four thyristor, single phase cycloconverter shown in Figure 1.1, but with the input split secondary transformer replaced by the split phase winding of the motor and each pair of thyristors replaced with a single triac. For positive bank operation, triac Q1 is triggered during the mains positive half cycle and Q2 is triggered during the mains negative half cycle. For negative bank operation, triac Q2 is triggered during the mains positive half cycle and Q1 is triggered during the mains negative half cycle.

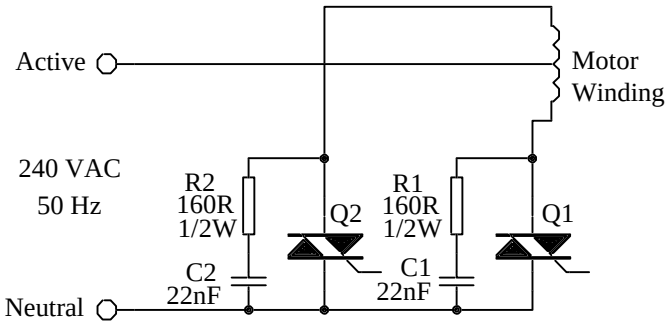


Figure 4.1 Complete power circuit for one phase of the cycloconverter

The triacs used are a high commutating dv/dt type supplied by SGS-Thomson. The high dv/dt reduces the size of the snubber components. Both type TXDV808 and the higher power TPDV1225 were used successfully in the prototype. The experimental tests described in this chapter were undertaken with the TPDV1225 triac in circuit. The triac ratings are as follows:

TXDV808:
I_{TRMS}: 8 A
V_{DRM}: ±800 V
dv/dt: 200 V/µs
$(dv/dt)_C$: 200 V/µs @$(di/dt)_C$ = 7 A/ms, 10 V/µs @$(di/dt)_C$ = 28 A/ms
Package: TO 220AB insulated

TPDV1225:
I_{TRMS}: 25 A
V_{DRM}: ±1200 V
dv/dt: 200 V/µs
$(dv/dt)_C$: 200 V/µs @$(di/dt)_C$ = 20 A/ms, 10 V/µs @$(di/dt)_C$ = 88 A/ms
Package: TOP 3 insulated

An important parasitic element of the circuit is the leakage inductance between the two halves of the split winding on each motor phase. This inductance limits di/dt on the triacs during commutation, provides RFI filtering, and gives some degree of protection to the triacs from mains transients. Note that this leakage inductance needs to be reasonably high. In the prototype motor, sufficient leakage inductance was achieved by winding the two winding halves of each phase as separate coils but placing them in the same slots.

The circuit has some important advantages in comparison to alternative converters using a DC link and PWM inverter. First, there is only one switching element in the current flow path for each phase at any one time, and this is a low voltage drop triac, giving a converter efficiency of around 99%. Next, the leakage inductance between the two winding halves of each phase of the motor provides RFI filtering for the triac switching noise. A separate RFI filter normally has to be added to a PWM inverter drive. Most importantly, the cost of the circuit, using only four low cost triacs, is considerably lower.

A disadvantage of the circuit is that the split phase motor windings reduce motor efficiency, requiring a larger motor size for the same power output. This could be overcome by using a bridge circuit of four triacs for each phase allowing a single winding to be used on each motor phase. This would require eight triacs though, with four triacs requiring isolated gate drives, adding considerably to the cost. A better solution is to use a single phase to three phase circuit using six triacs and a standard three phase motor. Such a circuit, using double integral control of the triacs, has been developed by Zhang [19].

4.2 Control Circuit

A block diagram of the control circuit and its connections to the power circuit are shown in Figure 4.2. The complete circuit is shown in Appendix B.

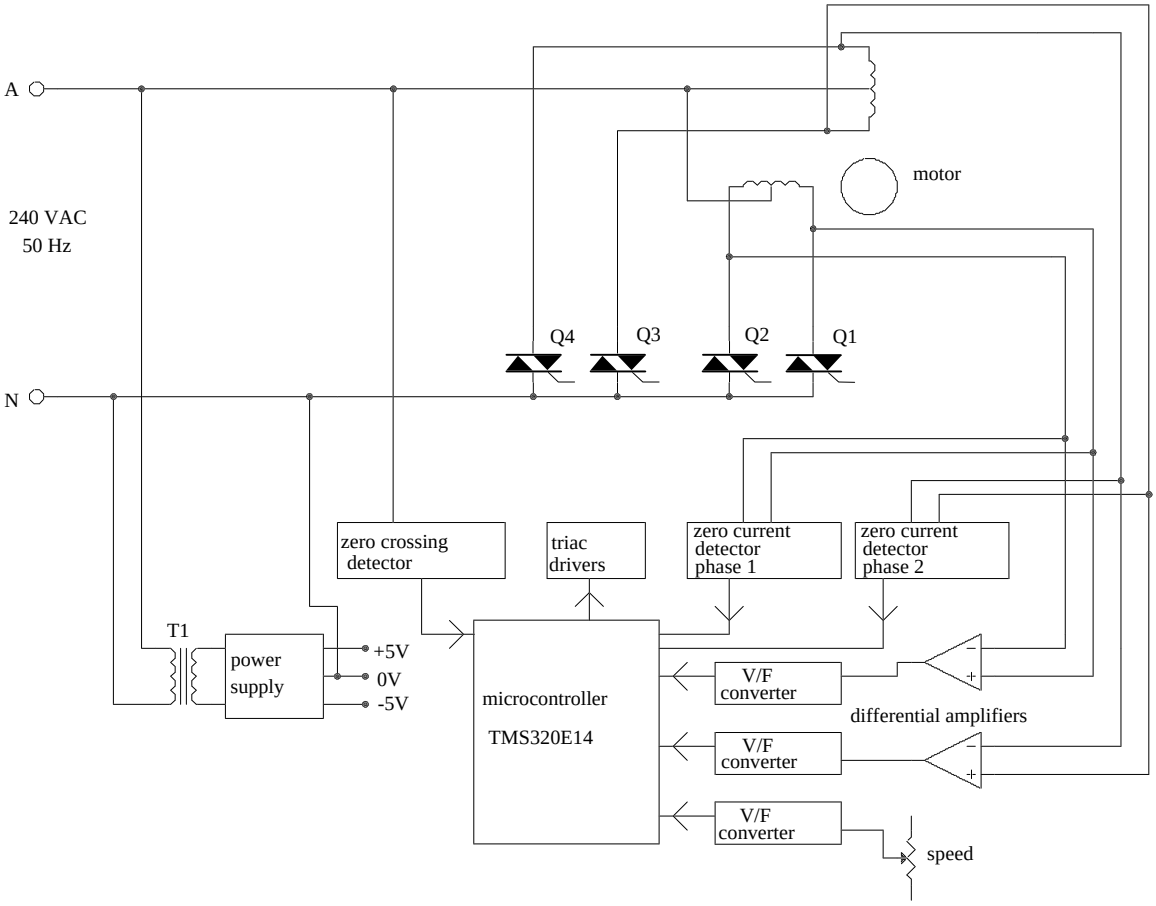


Figure 4.2 Block diagram of the control circuit together with a simplified power circuit.

The control functions are implemented with the digital signal processor based micro controller type TMS320E14 from Texas Instruments with a 24 MHz crystal frequency. This processor is fast enough to allow a sample rate of 45 times per half cycle. It was found from trial and error that this sample rate is the about the minimum that could be used to reduce torque harmonics resulting from the finite sample time steps to an acceptable level.

The output phase voltages are measured across the whole winding on each phase to achieve a balanced measurement. This is done using differential amplifiers (with high voltage inputs and a gain much less than 1) feeding into two low drift voltage to frequency converters with a frequency offset to allow both positive and negative voltage

measurement. The V/F converters are of the synchronous type timed off the micro controller's crystal clock to achieve the required low drift. They are built using discrete components rather than using a single chip V/F converter as this proved to be much cheaper. Their centre operating frequency is 27kHz which allows a wide enough swing in frequency to achieve the required accuracy. The outputs of the V/F converters are fed into two hardware counters in the TMS320E14 micro controller. The speed reference signal, which is read from a potentiometer, is also fed to the micro controller via a V/F converter which is a very simple low quality type.

The method of detecting zero current in each phase is to measure the voltage across each triac and assume the phase current is zero if the voltage across both triacs in the phase is greater than about 5V. This method was first proposed by Hamblin et al [18].

The micro controller interfaces to the triacs via simple buffer circuits connecting the micro controller's output ports to the triac gates. The triacs require a negative gate drive for maximum sensitivity, so the micro controller's power rails are connected to -5V and 0V to obtain a negative output from its ports.

4.3 Software

A block diagram illustrating the basic operation of the software is shown in figure 4.3. The complete software listing can be found in Appendix C.

An interrupt which starts the sample routine is generated 90 times per mains cycle by a 16 bit timer internal to the TMS320E14 microcontroller. The period of the timer is itself adjusted by a phase locked loop routine, running once per mains cycle, to keep the sample interrupts synchronised with the mains. The zero crossing detector supplies the phase information for this routine. A phase locked loop is used rather than other simpler techniques such as re-synchronising the timer at each zero crossing because it gives a more accurate positioning of the sample times as well as filtering the effects of noise on the zero crossing detector.

The sample routine contains the triac control algorithms. For each output phase, a check is made to see whether a change in banks is required, the main algorithm is calculated as per equation 3.23, and the correct triac is triggered if required. Various house keeping tasks are also performed here.

A more detailed description of the various sections of the software follows.

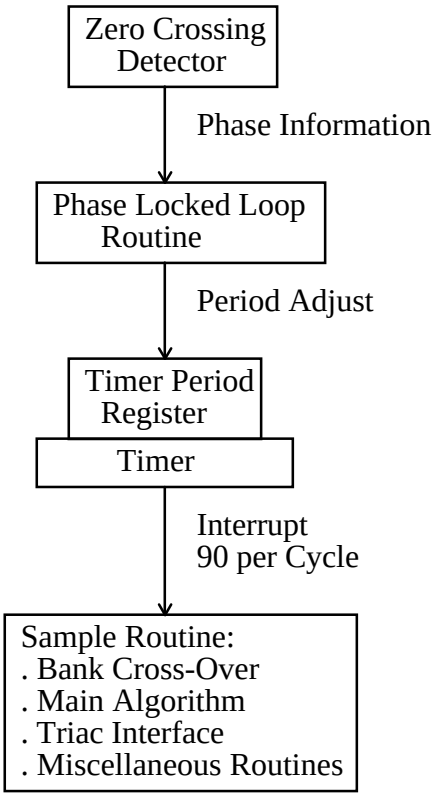


Figure 4.3 Block diagram of the software.

4.3.1 Phase Locked Loop

A detailed block diagram of the operation of the phase locked loop is shown in Figure 4.4. The phase locked loop itself is a conventional second order loop using a proportional integral compensator. The natural frequency of the loop is set to 1.0 Hz and the damping factor to 0.7.

The phase locked loop software adjusts the period of the interrupt timer for the sample routine so that exactly 90 samples per mains cycle is generated. To generate 90 samples per cycle for a mains frequency of 50 Hz, the timer period needs to be set to a nominal value of about 167 with the timer clock operating at its maximum frequency of 750 kHz.

One problem is that the timer period cannot be set to fractional values. Without some means of compensating for this, then with a phase locked loop response time of about 0.3 seconds and timer period error of 0.5, the sample positioning could be out by as much as 0.5/167 times 0.3 = 0.9 msec or 4 sample periods. This effect is compensated for by using a dithering routine which adjusts the timer period register every sample to obtain a long term timer period accuracy of 20 bits.

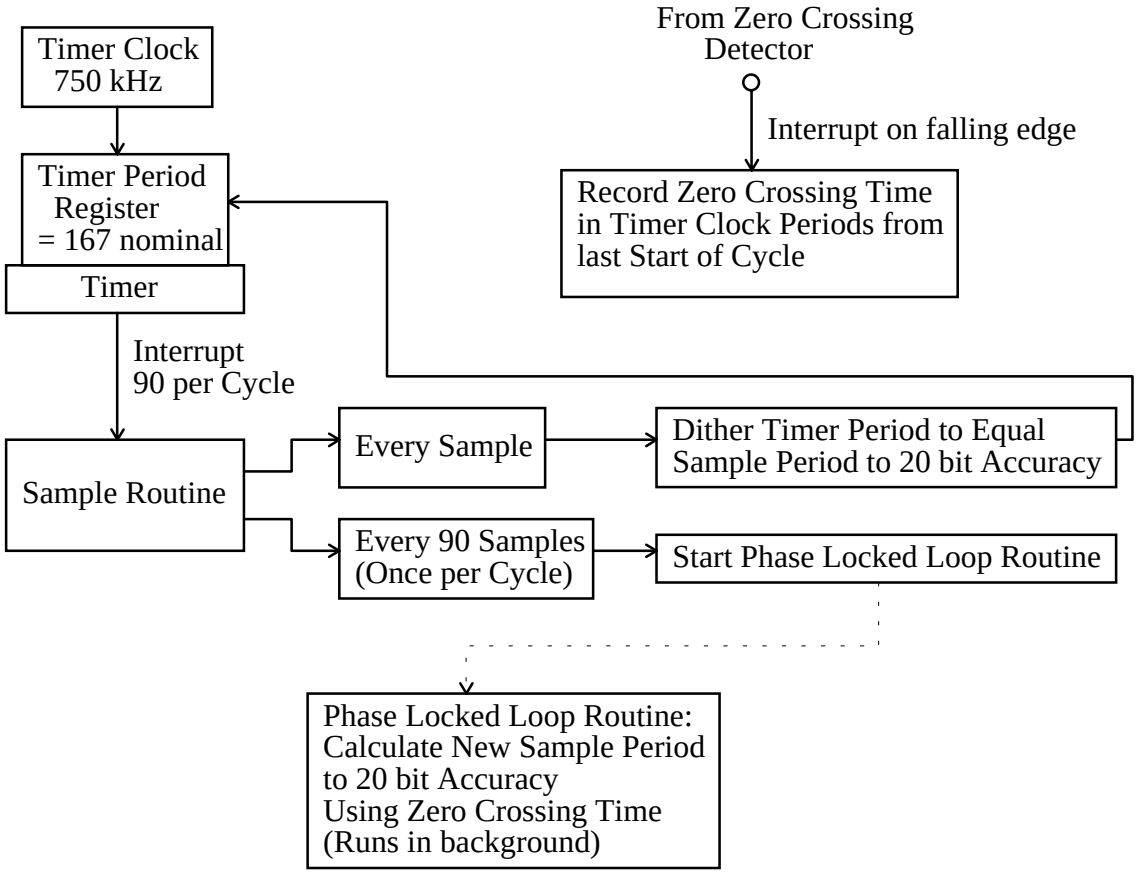


Figure 4.4 Block diagram of the phase locked loop operation.

The dithering routine is straight forward. The phase locked loop routine calculates the sample period to 20 bit accuracy with a fractional part of 16 bits once per cycle. The dither routine, which runs once every sample, takes this value and adds it to a 20 bit buffer register. The upper 8 bits of this register are used to update the timer period register for the next sample period then set to zero, whilst leaving the lower 16 bit fractional part unchanged. A slight modification made to this to make more efficient use of the 16 bit microprocessor is to calculate the change from the nominal base period rather than the 20 bit period itself. This change value can be conveniently stored in only 16 bits. Similarly the buffer register can also be reduced to only 16 bits, with the nominal sample period added only when the new timer period is being calculated.

The phase locked loop routine itself calculates the present phase error then applies proportional integral compensation to this to derive the new sample period. The phase error is calculated from the time of the last negative zero crossing of the mains which is recorded as the number of timer clock periods that have elapsed since the beginning of the mains cycle by an interrupt routine triggered by the negative zero crossing. The

negative zero crossing is chosen rather than the positive zero crossing because this occurs half way through a cycle when the computer is not so busy as at the start of a cycle. It also simplifies the phase shift calculations. The zero crossing interrupt routine has the highest priority to maximise the accuracy of the recorded time.

4.3.2 Tasks Carried Out by the Sample Routine at the Start of Each Half Cycle

At the start of each half cycle, which occurs every 45 samples, the sample routine must carry out the tasks which are listed in block diagram form in Figure 4.5 in addition to the normal jobs carried out every sample. Also shown in this diagram is the interrupt routine used to form a software V/F counter for the speed V/F converter.

Note that in the initiation of the numeric integrations for each phase, the integral of the boost voltage for the previous half cycle is subtracted from the output voltage V/F counter. This is to make the output V/F counter equal to the integral of v_o' as defined by equations 3.19 and used in equation 3.23. Also note that the $\int\int v_o$ register is initialised with only half of $\int v_o$ as required for trapezoidal integration.

The input phase register is used to keep track of the input phase in the form of the number of elapsed samples since the start of the half cycle. Here, this register is reset to zero.

The background jobs shown here take precedence over the phase locked loop background routine shown in figure 4.4.

4.3.3 Tasks Carried Out by the Sample Routine at Every Sample Except at the Start of Each Half Cycle

When a sample routine is not the start of a half cycle, then for each output phase until the triggering of the triac, the tasks of calculating the double integral algorithm as per equation 3.23, changing banks if required and triggering the triacs as required are carried out. A flow chart of these tasks is shown in Figure 4.6.

As shown, the tasks must be repeated for both the U phase and the V phase. Note that the main routine must check on various conditions before calling the double integral algorithm and triggering the triac.

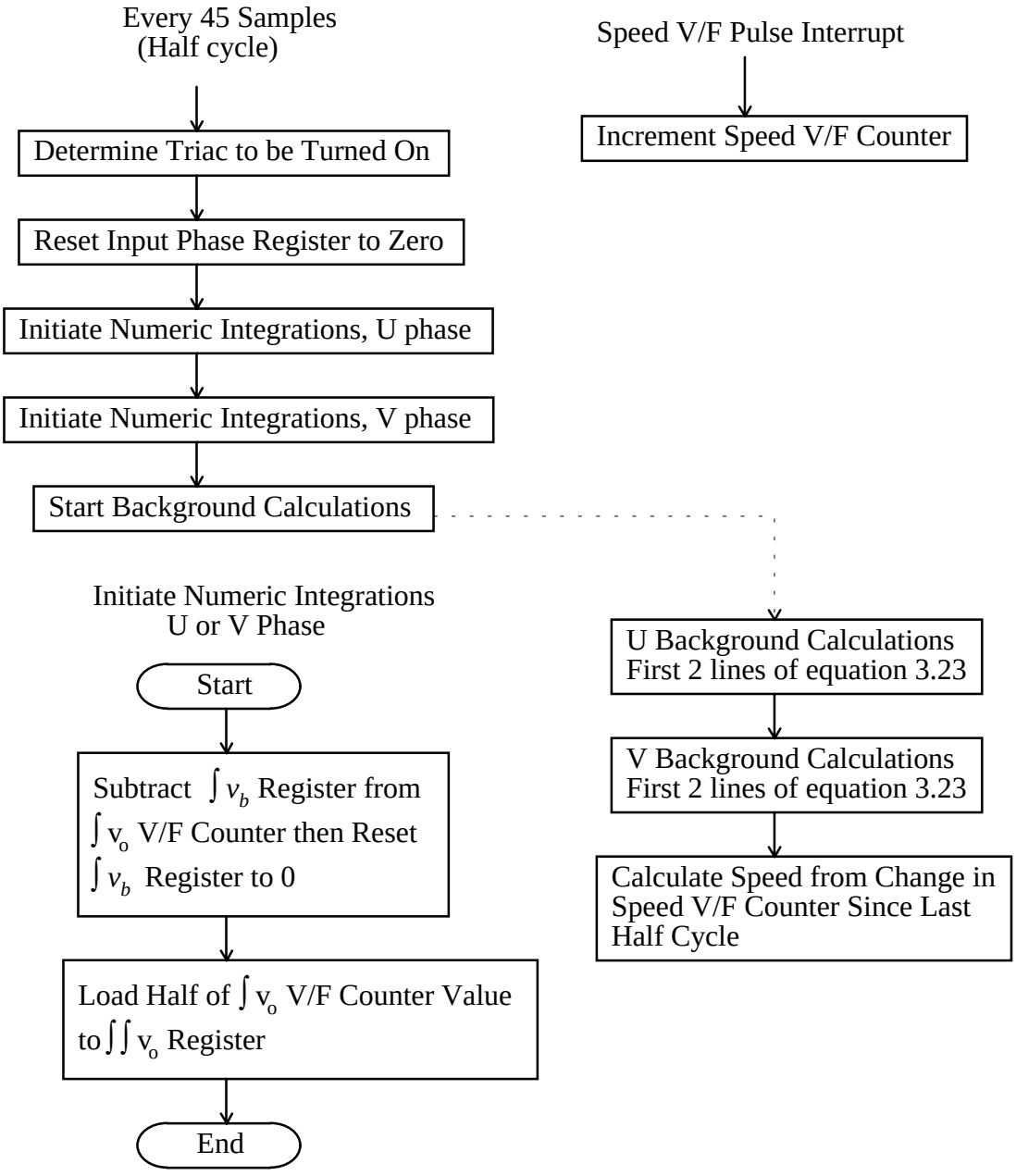


Figure 4.5 Block diagram of tasks carried out every half cycle sample and the related speed V/F software counter.

One of these is a check on the endstop. This is defined as the last sample in a half cycle in which the triac can be triggered to ensure that the previous on triac is commutated off. If this endstop is reached, the next triac is immediately triggered on.

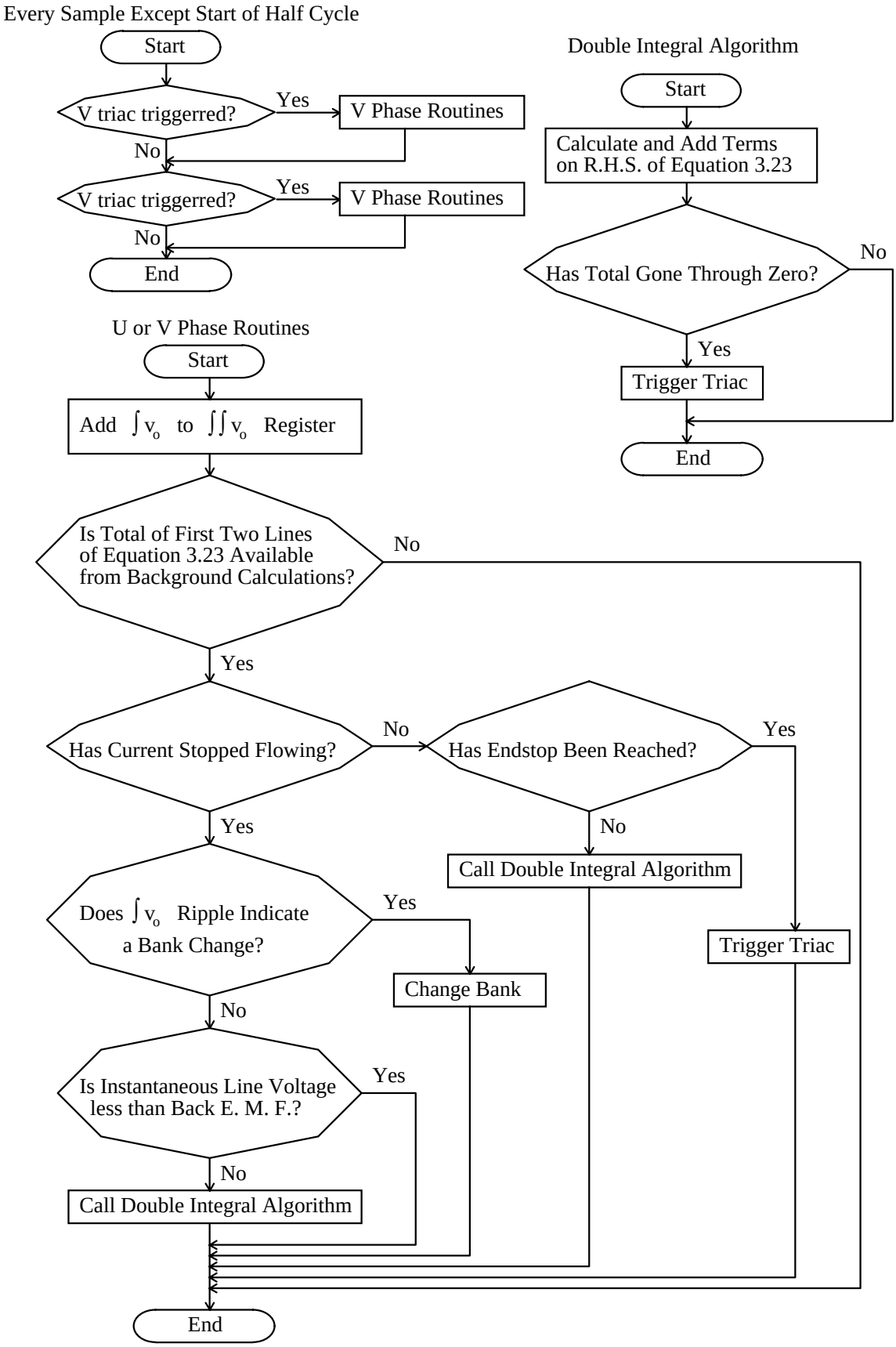


Figure 4.6 Tasks carried out at every sample except at the start of a half cycle.

Another check which is carried out if the previous triac is turned off, is to test if the line voltage applied to the next triac is less than the motor back e.m.f. If this is the case, the triac must not be turned on or it will conduct in the wrong direction. The back e.m.f. is calculated from the output frequency, with a margin added of safety. An alternative method is to measure directly the voltage polarity across the triac, although the software method used here was found to work well.

Note that the double integral of v_o is effectively evaluated to half way through the sample interval by not halving the final value of $\int v_o$ added to it. This more closely matches the actual triac trigger time which is delayed due to the time required to do the calculations.

The change bank section of the program is quite lengthy as it involves a readjustment of the results from the background calculations and the selection of the triac to be triggered next. For this reason, no attempt is made to evaluate the double integral algorithm in the same sample as a bank change over.

4.3.4 Tasks Carried Out by the Sample Routine at Every Sample

The tasks undertaken at every sample routine are miscellaneous house keeping tasks. They are listed in figure 4.7.

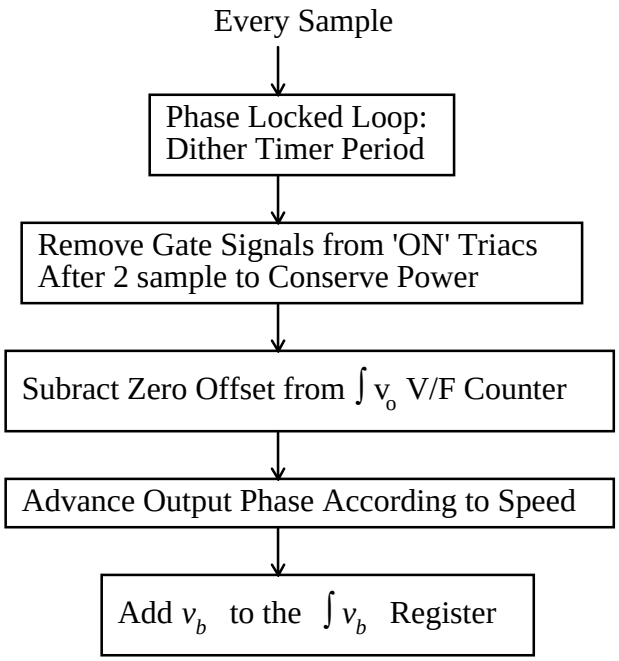


Figure 4.7. Tasks carried out every sample routine.

4.3.5 Sample Routine Program Flow

A flow chart showing the approximate program flow of the sample routine is shown in Figure 4.8.

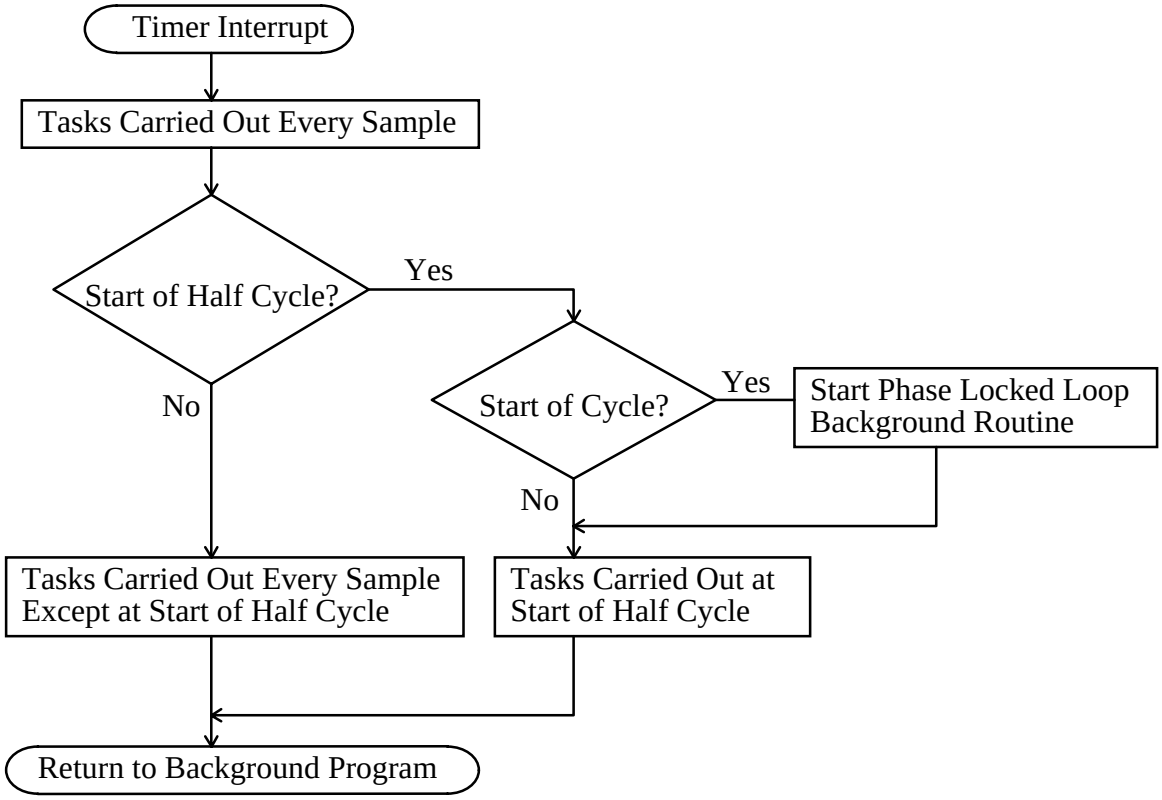


Figure 4.8 Flow chart of the sample routine.

4.3.6 Initialisation

To start the cycloconverter, several initialisation tasks have to be carried out. These include initialising all the variables, adjusting the DC offsets of the voltage to frequency converters and starting the phase locked loop. These tasks are shown in Figure 4.9.

Note that the phase locked loop period is initialised to the mains period, measured precisely over eight periods. This, together with starting the phase locked loop in synchronism with the mains, minimise starting transients in the phase locked loop which may otherwise cause it to jump out of lock. No method of detecting and correcting out of lock conditions have been incorporated in the software nor is it necessary since this could only occur with a mains outage which would cause a general reset anyway.

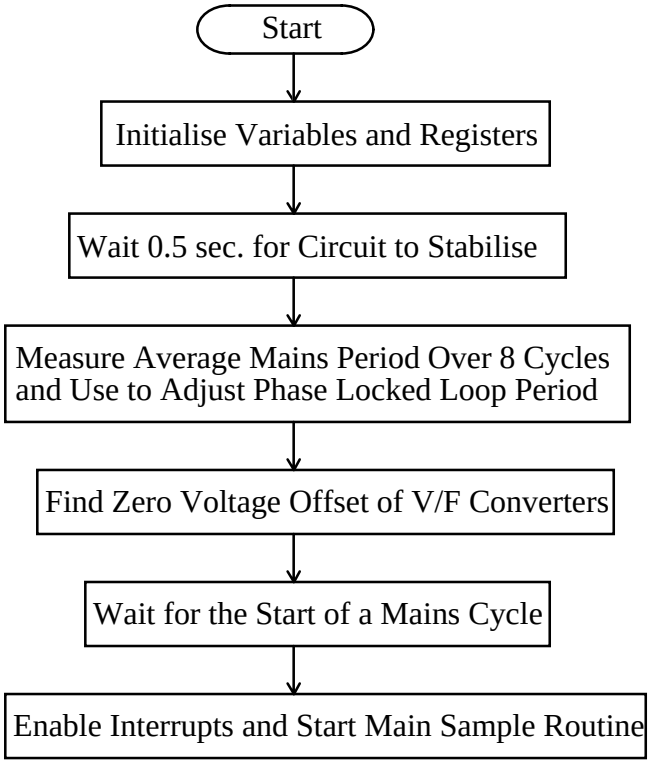


Figure 4.9 Initialisation routine.

Also note that the frequency offset of the V/F converters is recorded to be used later for correcting this. This eliminates the need to manually adjust these offsets.

4.4 Tests with a Motor Load

4.4.1 Motor Characteristics

The motor used for the tests is a specially wound two phase induction motor supplied by the industrial sponsors for this research, Brook Crompton Betts Pty Ltd. The motor rotor and stator laminations are from a single phase, 50 Hz, two pole, capacitor run induction motor rated at 700W. The motor stator has two windings on each phase which can be connected as a centre tapped winding as required.

Locked rotor and no load tests were conducted to determine the motor parameters. For the no load tests, no two phase sinusoidal supply was available, so the motor was supplied from the cycloconverter at an output frequency of 12.5 Hz and the magnetising inductance was derived from the fundamental components of voltage and current as measured with a Hewlett Packard 3582A spectrum analyser. The parameters were measured for each of the four windings then averaged. The locked rotor tests were

conducted at a current of 1.5 A using a 50 Hz supply. A table of the motor parameters, referred to one stator winding, and assuming the leakage inductance is split equally between the stator and the rotor, are listed in Table 4.1. The tests were taken at a motor temperature of 20°C.

Table 4.1 Motor parameters for the two phase, four winding motor, referred to one stator winding, at a motor temperature of 20°C.

Stator Resistance, R_1	15Ω
Rotor Resistance, R_2	11Ω
Stator Leakage Inductance, L_1	35 mH
Rotor Leakage Inductance, L_2	35 mH
Magnetising Inductance, L_m	1.5H

It was found after initial running tests of the motor with the cycloconverter that, due to the low motor leakage inductance, the motor harmonic current was excessive. This was corrected by adding extra series inductance external to the motor. An extra 100 mH was added to each phase using the circuit shown in Figure 4.10. An alternative is to increase the motor leakage inductance itself by changing the design of the motor laminations. The extra cost of a motor with increased leakage inductance would be minimal for large production quantities. A detailed analysis of the optimum size of the leakage inductance for a given motor size was conducted by J. Zhang [19].

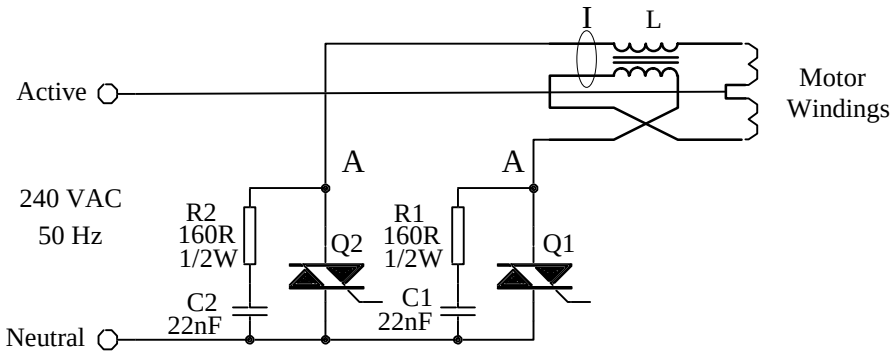


Figure 4.10 Addition of an extra inductor, L, to increase the effective motor leakage inductance. Nodes AA are the measurement points for phase voltage measurements and loop I shows the current probe connection to measure total phase current.

4.4.2 Equipment Setup for Load Tests

To test the cycloconverter and motor under load, the motor was coupled to a separately excited DC motor/generator which in turn was loaded with power rheostats. The name plate ratings of the motor/generator, specified for motor operation, are as follows:

Speed: 3450 rpm
Power Output: 0.57 kW
Field Voltage: 230V
Field Current: 0.3A
Armature Voltage: 230V
Armature Current: 3.1A

During all tests, the field current was kept at rated value.

To measure torque, the DC motor/generator torque verses armature current characteristic was measured statically using an extension arm locked to the rotor and spring balances. The torque constant was measured at 0.60 Newton meters per Ampere.

Other equipment used include a Yokogawa DL1200A oscilloscope for waveform recordings, a Hewlett Packard 3582A spectrum analyser and a Tektronix A6303 current probe with an AM503 current probe amplifier. Waveforms from the oscilloscope and the spectrum analyser were down loaded to a personal computer via a GPIB cable for plotting.

Also recorded during load tests are the flux feedback and reference waveforms internally generated by the microprocessor. This data is picked up from the microprocessor with a logic analyser then sent to a personal computer for plotting.

4.4.3 No Load Tests

The voltage and current waveforms on the output of one phase of the cycloconverter were recorded at various frequencies with no load on the motor. These are shown in Figures 4.11 to 4.14. These are measured at the locations shown in the circuit of Figure 4.10. The voltage is measured across both motor windings in series and so is twice the motor phase voltage. The measured current is the addition of the currents in the two phase windings. This is the actual motor phase current. For these tests, the internal flux reference table used by the microcomputer is set for 120 V rms at 25 Hz and the boost

voltage is set to produce 3.8 V rms at a phase angle of 90° lagging from the component of the output voltage generated from the flux reference. This overcomes the voltage drop across the stator resistance due to the magnetising current.

Figure 4.11 shows the output waveforms at a frequency of 5 Hz. The smoothness of the current waveform envelope shows the excellent ability of the double integral modulation method to cope with severe discontinuous current situations. Also note the accuracy of the change-over between the positive and negative banks.

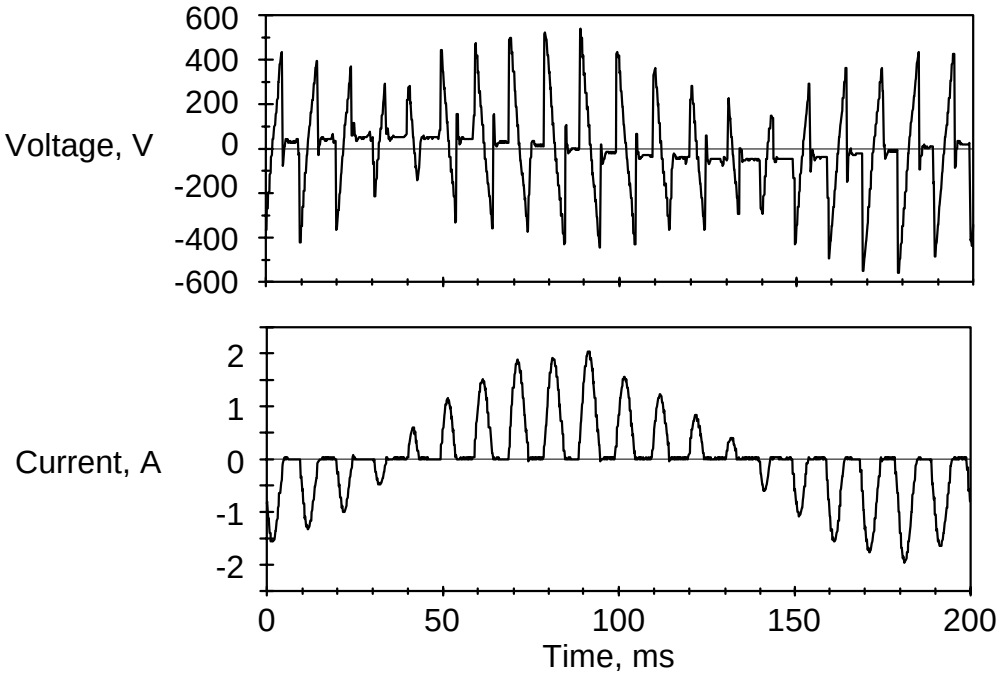


Figure 4.11 Output voltage and current waveforms for one motor phase of the 2 phase cycloconverter at 5 Hz with no load. The voltage is measured across both windings on the phase (and is thus twice the nominal phase voltage) and the current is the sum of the currents in both windings.

Figures 4.12 to 4.14 show operation at 20 and 25 Hz. Two sets of waveforms at different input to output phase relationships are shown for 25 Hz in Figures 4.13 and 4.14. In Figure 4.13, there are two current pulses per output half cycle, but they occur at each end of the half cycle, requiring them to have a large amplitude to generate the fundamental component of the current. As the load on the motor is increased, the amplitude of these current pulses must be increased further, but as can be seen in Figure 4.13, there is no room to advance the trigger angle for the first pulse in the half cycle as it must wait till the previous current pulse in the opposite bank is finished and bank change-over has been completed. This puts a limit on the maximum torque that can be

obtained from the motor at 25 Hz before phase control is lost. In Figure 4.14, there is only one current pulse per half cycle, but it occurs at the centre of the half cycle and so does not have to be very large to generate the required fundamental component of the current. Thus, operation at 25 Hz at full load can only occur with the input and output phases locked. Variable frequency operation at full load up to 20 Hz has been found possible, but performance deteriorates above this frequency. An increase in the maximum output frequency can be obtained by using a single phase to three phase cycloconverter drive as developed by J. Zhang [28,30,31].

As a further indication of the performance of the double integral control method, a plot is made of the rms value of the fundamental component of the output voltage as measured with the spectrum analyser versus output frequency in Figure 4.15. The internal flux table reference used by the microprocessor is set to 120 V rms at 25 Hz and voltage boost is turned off. The ideal voltage versus frequency curve for this set up is superimposed on the graph for comparison. The amplitude of the fundamental component is kept close to the set point value at all frequencies including 25 Hz.

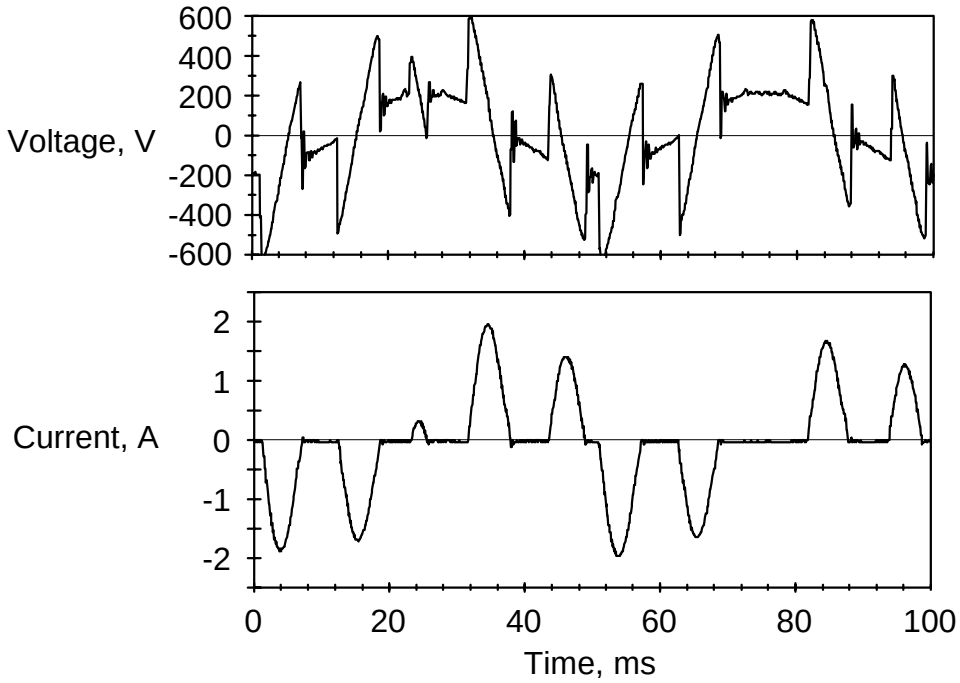


Figure 4.12 Output voltage and current waveforms for one motor phase of the 2 phase cycloconverter at 20 Hz with no load.

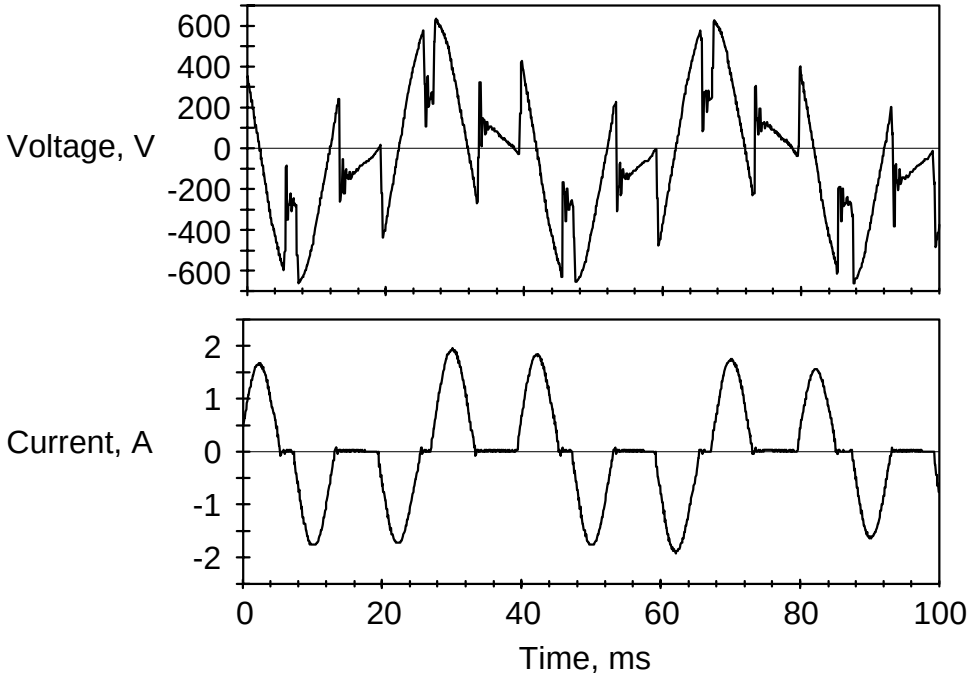


Figure 4.13 Output voltage and current waveforms for one motor phase of the 2 phase cycloconverter at 25 Hz with no load.

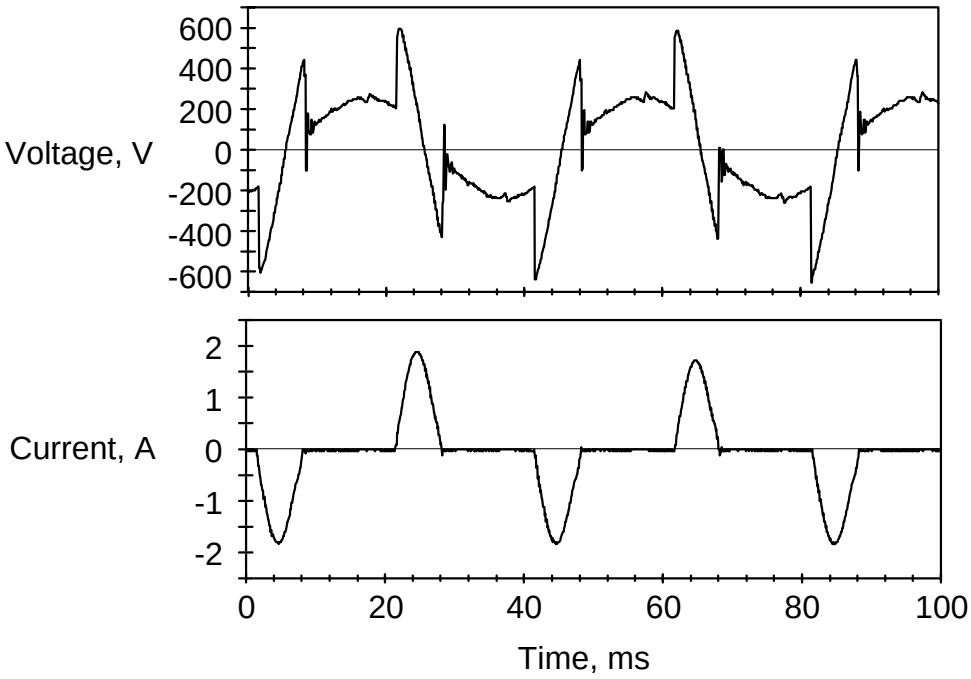


Figure 4.14 Output voltage and current waveforms at 25 Hz with a different input to output phase relation to Figure 4.13.

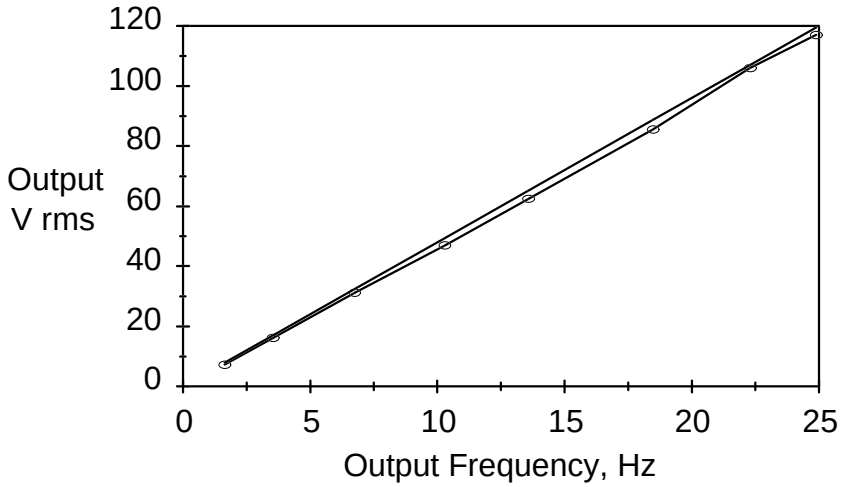


Figure 4.15 Fundamental component of output voltage against output frequency with the ideal straight line value included for comparison.

4.4.4 Load Tests

In this section, the results of load tests at output frequencies of 6 Hz and 20 Hz are described and illustrated. Included in the tests are the input current waveform and harmonic spectrum and the output voltage and current waveforms and harmonic spectrum. These tests were conducted with the reference flux of the cycloconverter increased to give 140 V at 25 Hz to help overcome the voltage drop across the extra motor inductance. Also, a quadrature voltage boost of 3.8 V rms is applied as for the no load tests. An in phase component of voltage boost could also be added to compensate for the stator voltage drop due to load current, but this extra complication has not been implemented here. A more complete performance analysis together with parameter optimisation and a simulation can be found in Zhang [19,27].

The 6 Hz tests were conducted at a motor load of 0.9 Nm, which is the maximum load torque which could be obtained at this frequency with the experimental set-up. The resulting voltage and current waveforms for one output phase are shown in Figure 4.16. The voltage is measured across both phase windings in series as for the no load tests. Also shown in Figure 4.17 is the frequency spectrum of the output current. Apart from the 6 Hz fundamental, the only significant components are the two 100 Hz sidebands at 94 and 106 Hz.

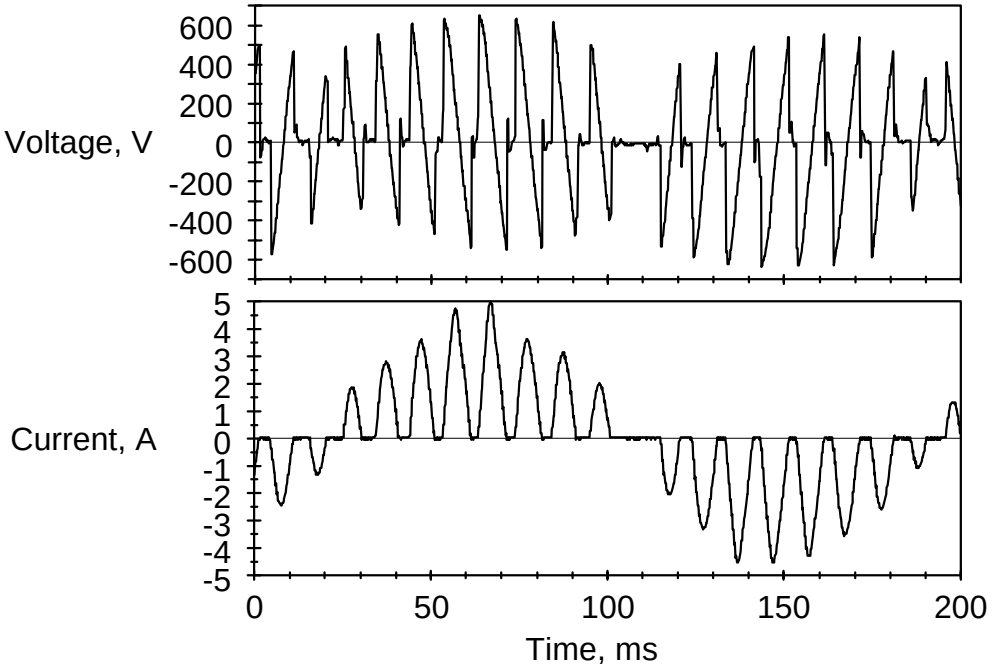


Figure 4.16 Output waveforms for one phase of the 1 to 2 phase cycloconverter operating at 6 Hz with a motor load of 0.9 Nm.

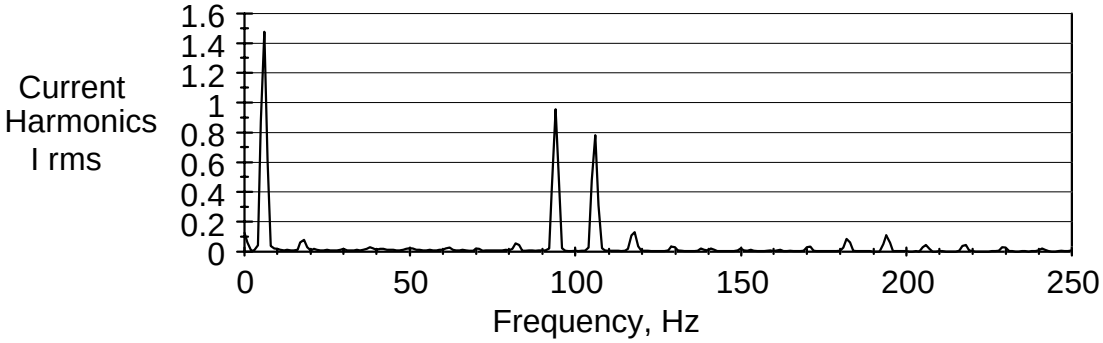


Figure 4.17 Frequency spectrum of the output current with 6 Hz output frequency.

Shown in Figure 4.18 are the output voltage and current waveforms at 20 Hz for a motor load of 1.4 Nm. The frequency spectrum of the current waveform is shown in Figure 4.19. Again, the only significant components apart from the fundamental are the sidebands of 100 Hz, particularly the lower sideband at 80 Hz which is of increased amplitude because of the lower impedance of the motor inductance at this frequency.

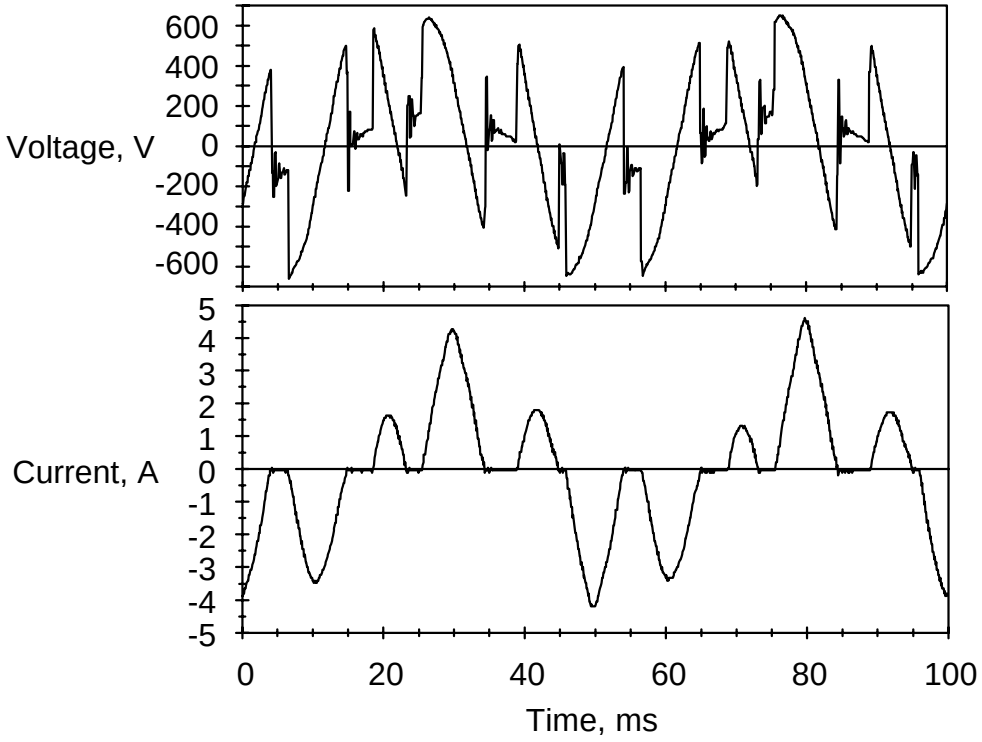


Figure 4.18 Output waveforms for one phase of the 1 to 2 phase cycloconverter operating at 20 Hz with a motor load of 1.4 Nm.

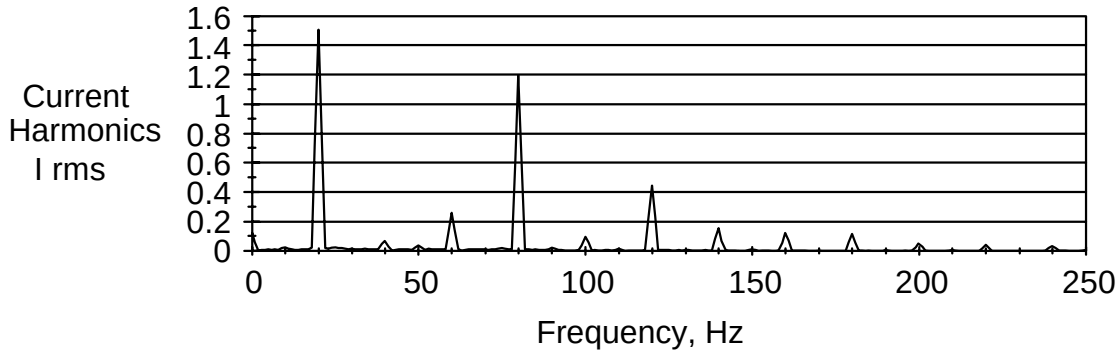


Figure 4.19 Frequency spectrum of the output current with 20 Hz output frequency.

Of growing concern these days are the harmonics injected into the mains supply by motor drives, with tighter regulations on harmonics being introduced in most countries. The input current waveform and its spectrum for this drive under load for output frequencies of 6 Hz and 20 Hz are shown in Figures 4.20 to 4.23. The input current harmonics are very low and would easily meet the new IEC 555-2 standard.

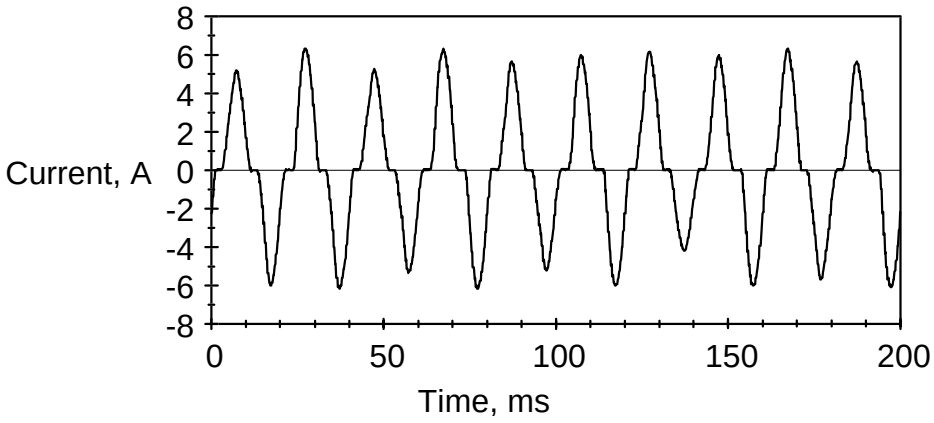


Figure 4.20 Input current waveform for the 1 to 2 phase cycloconverter operating at 6 Hz with a motor load of 0.9 Nm.

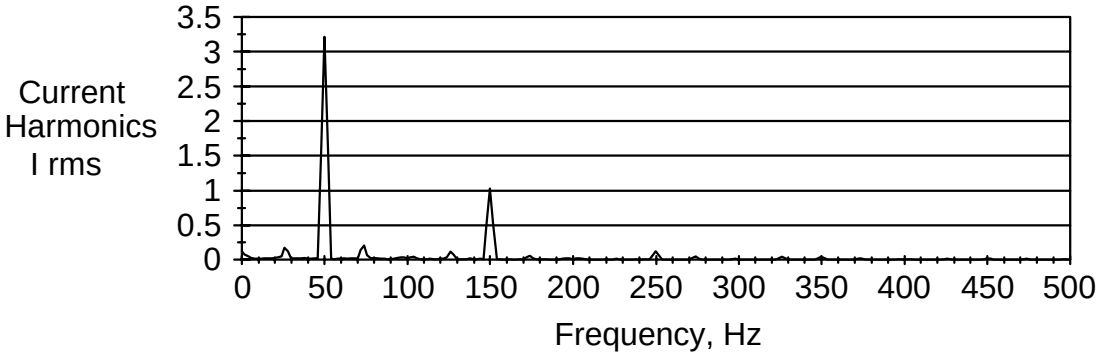


Figure 4.21 Frequency spectrum of the input current with 6 Hz output frequency.

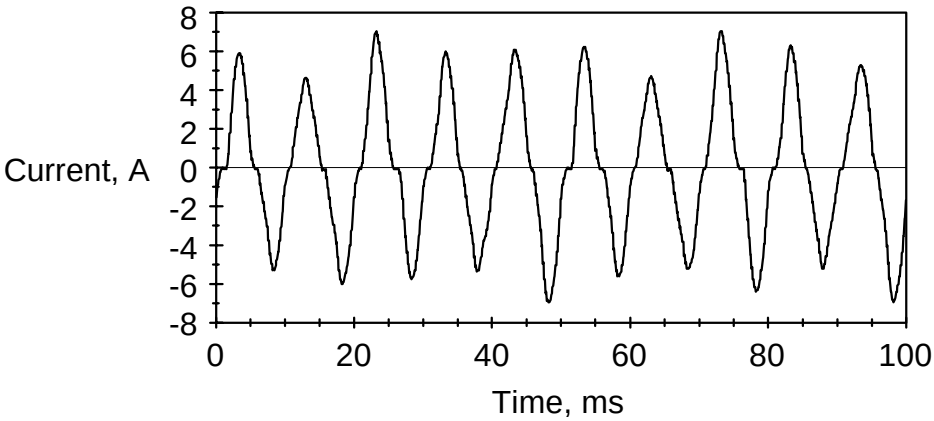


Figure 4.22 Input current waveform for the 1 to 2 phase cycloconverter operating at 20 Hz with a motor load of 1.4 Nm.

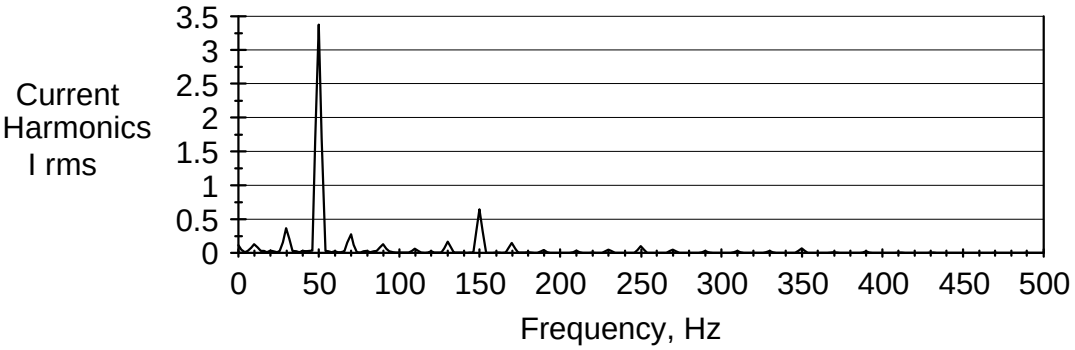


Figure 4.23 Frequency spectrum of the input current with 20 Hz output frequency.

4.4.5 Feedback Flux Waveforms

An indication of the performance of the double integral control algorithm can be gained from inspection of the reference and feedback flux waveforms as used in the microcomputer. These are shown in Figures 4.24 and 4.25 for 6 Hz and 20 Hz output frequencies with the motor under load. The data for these waveforms was collected from the microcomputer with a logic analyser. These waveforms illustrate the ability of the double integral control method to keep the feedback flux close to the reference flux even at high output frequencies.

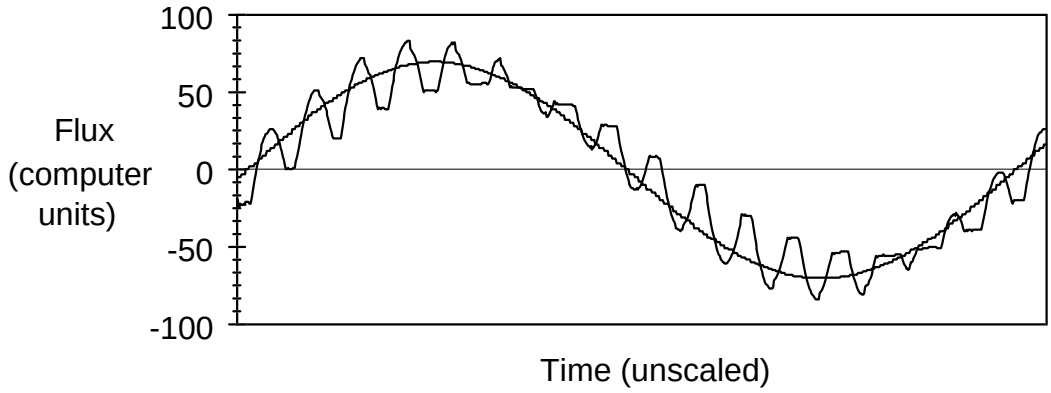


Figure 4.24 Computer derived output and reference flux waveforms for operation at 6 Hz and 0.9 Nm load.

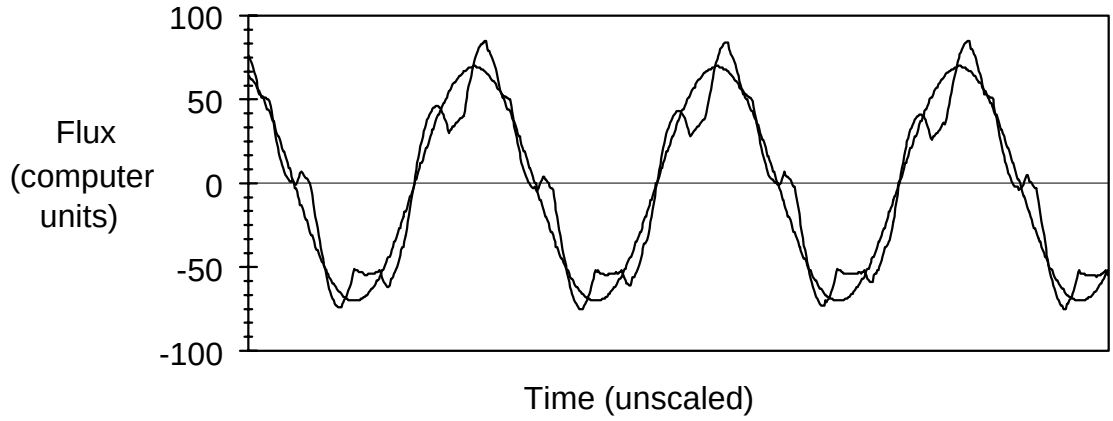


Figure 4.25 Computer derived output and reference flux waveforms for operation at 20 Hz and 1.4 Nm load.

5. THE 3-PHASE, 3-PULSE SCR CYCLOCONVERTER DRIVING A 3-PHASE INDUCTION MOTOR

Commercial 3 phase cycloconverter motor drives, with their 36 thyristor, 6-pulse circuits with input isolation transformers, are too expensive except for specialised applications. The 3-pulse cycloconverter is low enough in cost for general purpose use, particularly where regeneration is required, as it has only 18 thyristors and does not require transformers, but the performance with conventional modulation techniques is inadequate. The use of double integral control corrects this problem and, as can be seen from the test data in this section, results in a performance which in some areas is comparable to that of the conventional 36 thyristor 6-pulse cycloconverter.

5.1 The Power Circuit

The power circuit of the 3-pulse cycloconverter is shown in Figure 5.1. The circuit is conventional, except for the addition of the 75 microhenry saturating inductors on the output of each of the positive and negative thyristor banks. These inductors isolate the 'off' thyristors from the dv/dt produced by a thyristor turning on and greatly reduce the size of the RC snubber required on each thyristor. The 9 microhenry input inductors limit the thyristor di/dt and provide some e.m.i. suppression.

The specifications for the thyristors used are as follows:

Type: Semikron SKKT26/12E (two thyristors per module)
Max. Current: 50A rms, 25A av.
Max. Forward and Reverse Voltage: 1200V
Max. dv/dt: 1000V/us

5.2 The Control Circuit

A block diagram of the control circuit is shown in figure 5.2. It is similar in form to the one to two phase cycloconverter, although the circuits have been completely redesigned to meet the higher demands of the three phase drive. The detailed schematic diagrams of the control circuit can be found in Appendix D.

The most critical parts of the control circuit affecting drive performance are the V/F converters. These are monolithic type AD650 from Analogue Devices, chosen for their very low drift and high linearity. These two parameters are important because they

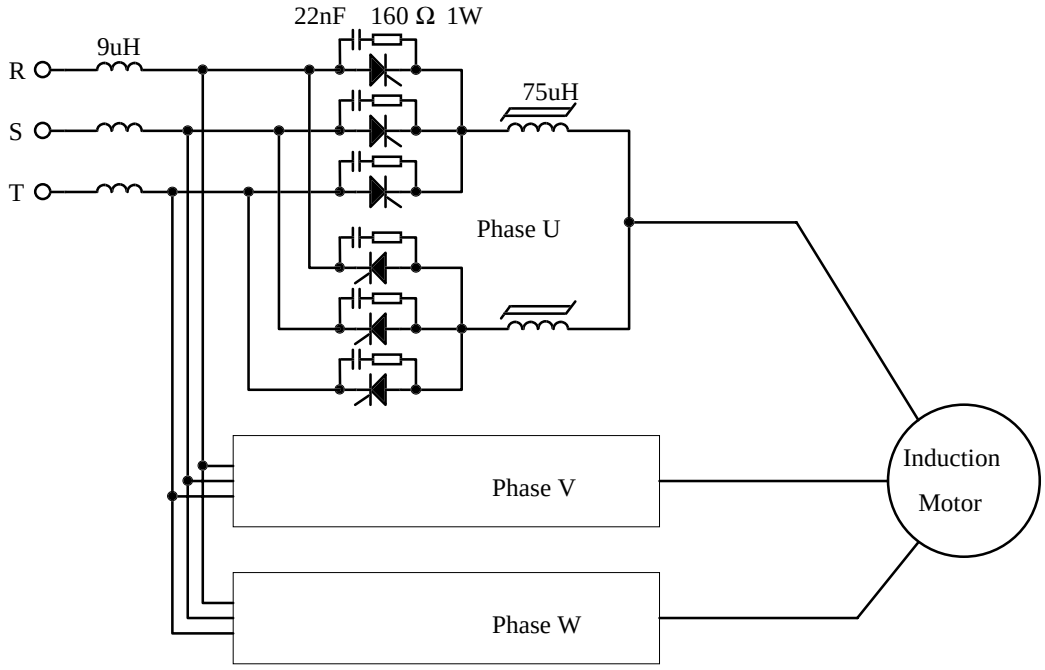


Figure 5.1 Power circuit of the 3-pulse cycloconverter

determine the residual D.C. voltage on the outputs which cannot be compensated by the feedback loops. This voltage must be kept very small to prevent significant D.C. currents in the stator of the motor. For instance, the motor used for testing has a stator resistance of only 0.3 Ohms. To keep the D.C. current down to an acceptable level of about 0.5A maximum for this motor, the maximum phase to neutral D.C. voltage that can be applied is 0.15 Volts. As well as this requirement, the input range for each V/F converter needs to extend to ± twice the peak nominal supply voltage, or about ± 700V in this instance, to ensure the converters never over-range. Thus the converters must handle a span of 1400V while producing a maximum offset of 0.15V. The type AD650 V/F converters easily meet this requirement without being expensive. For larger motors with even more stringent requirements, it would be necessary to add current feed-back to reduce D.C. currents to acceptable levels.

To enable bipolar operation, each V/F converter has a D.C. bias added to its input. This is derived from a precision voltage reference. Also, the reference point which the output voltages are measured with respect to is not the input neutral as is normally used but the centre point of the output of a full wave three phase bridge rectifier. The reason for this will be explained in the next section.

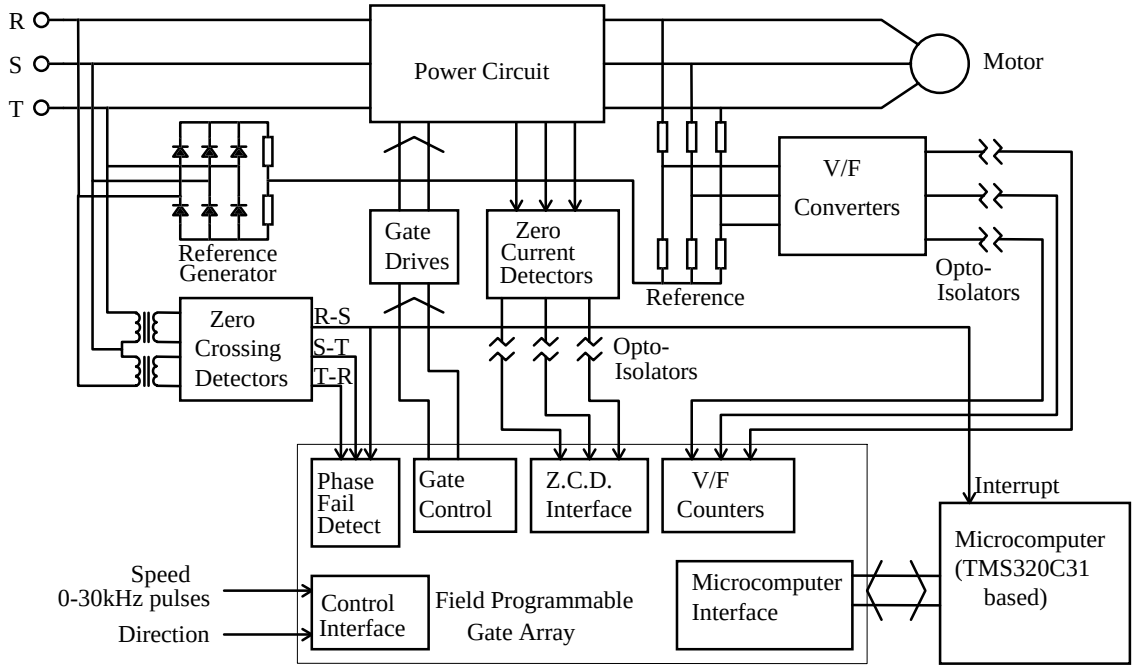


Figure 5.2 Block diagram of the control circuit of the 3-pulse cycloconverter.

The zero current detectors use the same technique to measure zero current as used in the one to two phase cycloconverter. The voltage across each thyristor in a phase is measured and when all the voltages are outside the normal "on" voltage range of the thyristors, a zero current is indicated.

The gate drive circuits use pulse transformers but are of an unusual design. Normally, pulses are sent to the gate of a thyristor about every 100 microseconds when it is on. When the thyristor is first turned on, the snubber supplies the holding current to the thyristor between gate pulses until the load current builds up. With the present design, the snubbers are too small to fulfil this function. Instead, the gate drive circuit shown in Figure 5.3 is used. In this circuit, the gate pulses are on for 5 μs and off for 1 μs. This off time is too short for the gate charge in the thyristor to dissipate, so the thyristor is effectively receiving a D.C. gate signal. The capacitor in series with the current limiting resistor provides a boosted gate current when the thyristor is first turned on to improve the thyristor's di/dt rating.

To synchronise the microcomputer with the mains and to check for phase failure or reversal, zero crossing detectors generate logic level square waves corresponding to the polarity of the voltages between phases R-S, S-T, and T-R. To check for phase failure or reversal, the relative timing between the three signals is checked and the cycloconverter is shut down when the relative timing is found out of tolerance.

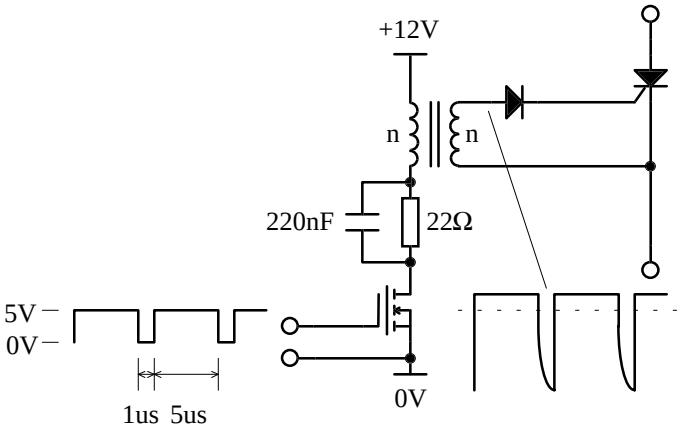


Figure 5.3 Gate drive circuit and waveforms.

The external controls for the drive are speed and direction. The speed input is a 0 to 30 kHz pulse input which sets the cycloconverter output frequency to 1/1000 times this input frequency. For the testing of the drive, the speed input pulses were generated by a function generator. The direction input is a logic compatible high for forward and low for reverse.

To process the input and output signals and to interface these to the microcomputer, a 1200 gate field programmable gate array, type A1010A made by Actel, is used. This is connected to the microcomputer's address and data lines and each module in the gate array is mapped to a part of the address space of the microcomputer. The detailed logic diagrams for the gate array can be found in Appendix E. It has been found that the combination of the field programmable gate array and the DSP base microcomputer is a very powerful method of implementing the control logic. The gate array allows the implementation of peripheral logic circuits such as timers, buffers and counters in the optimum configuration for the system and allows the interface to the microcomputer of the control functions to be done in a way which minimises software overheads.

The microcomputer consists of a Texas Instruments TMS320C31 32 bit floating point digital signal processor with associated ROM, RAM and interface logic operating at a crystal frequency of 24 MHz. This processor was chosen because it is powerful enough to allow most of the software to be written in "C".

5.3 Control Methods

The control methods used for the three phase cycloconverter are basically the same as those used for the single phase to two phase cycloconverter, but with some refinements added which are described in detail in this section. Advantage is taken of the increased computing power to use a version of the double integral algorithm with higher dynamic performance and higher accuracy. Also, as discussed in Section 3.4, the interaction between phases must be considered when determining the bank cross-over time.

5.3.1 Double Integral Algorithm

In order to allow current feedback and vector control to be easily added later on, the full double integral algorithm without approximations, using equation 3.17 in Section 3.2.2, which allows fast changes to the voltage boost vector was implemented. The full details of how this algorithm is implemented in practice is described in Section 3.2.2. For the research in this thesis, neither current feedback nor vector control are implemented and so the in-phase and quadrature components of the voltage boost are set to fixed values which can be adjusted only by re-compiling the software.

5.3.2 Input Reference

Normally the input reference voltage with respect to which all the input and output voltages are measured is the input neutral point, but for the three phase cycloconverter any voltage waveform can be chosen as the reference point. The actual voltage reference waveform chosen and how it is derived is shown in Figure 5.4.

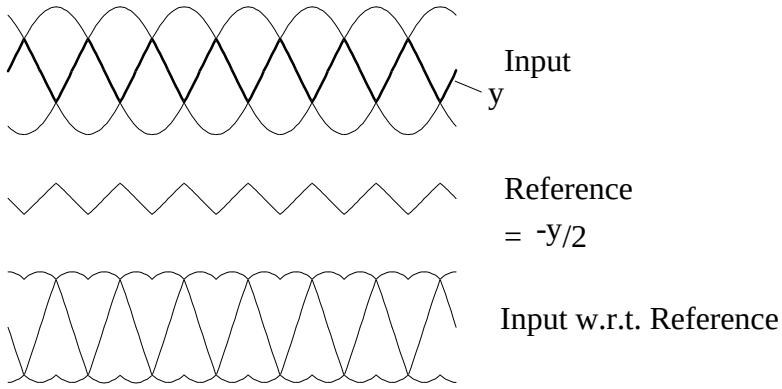


Figure 5.4 Derivation of the input reference voltage.

There is no strong advantage in choosing this reference over others, such as the actual input neutral point, but it does have the advantage of allowing the input with respect to this reference to be able to be approximated by a trapezoidal waveform, which simplifies the calculation of the end times of the trigger periods, found from the intersection of the output reference with the input waveforms. Also, it is easy to physically generate this reference waveform using a three phase bridge rectifier with a centre tapped resistor load as shown in Figure 5.2. Alternatively, the input neutral could be used, either directly or synthesised from star connected resistors, and the input reference subtracted in software.

Note that the maximum positive or negative output voltage with respect to either the input neutral or the new reference is $3\sqrt{3}/2\pi$ or 0.827 times the peak line to neutral input voltage.

5.3.3 Output Reference

The output reference is defined here as the wanted output voltage, v_r. The output reference voltage waveform must be chosen carefully as it affects the performance of the cycloconverter.

The only necessary requirement for the output waveforms is that the line to line voltages be sinusoidal and of the correct amplitude and phase. There is no requirement on the choice of the common mode voltage. One possibility is sinusoidal outputs with zero common mode voltage as shown in Figure 5.5(a). This is not ideal though, because the peak to peak excursion of the output voltages is 15.5% higher than the peak line to line voltage. For a given mains input voltage, this limits the maximum line to line output voltage from what it could be by the same percentage. Another possibility is to use the waveform of figure 5.5 (b) which is the same as the input waveform of figure 5.4, but this waveform is not smooth and has unnecessarily large dv/dt rates in parts of the waveform which may increase line to line voltage distortion at high frequencies when the phase controller attempts to follow the reference. The waveform chosen as a good compromise is that of Figure 5.5 (c). This waveform has a third harmonic sinusoidal common mode voltage of one sixth the line to neutral voltage, which is just enough to give a peak voltage the same as the peak line to line voltage.

With this output waveform, the peak output phase voltage is $2/\sqrt{3}$ times the peak output voltage. From the previous section, the peak output voltage is $3\sqrt{3}/2\pi$ times the peak

input phase voltage, so the maximum output voltage of the 3 phase cycloconverter is $3/\pi$ or 0.954 times the input voltage.

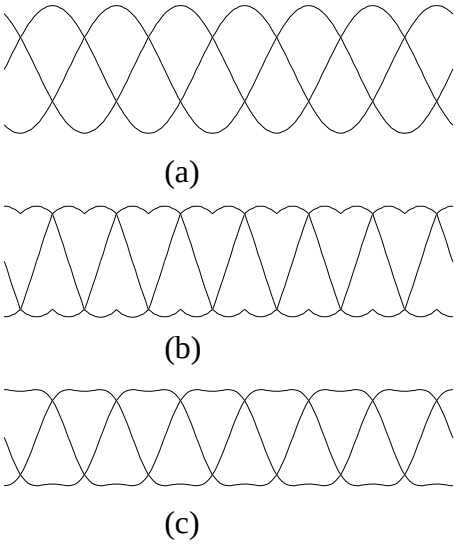


Figure 5.5 Possible waveforms for the output reference. Waveform (a) limits the peak line to line voltage, while waveform (b) has excessive dv/dt. The waveform chosen is (c).

The actual double integral control algorithm, using equation 3.17, requires the integral of the output reference for the flux component, rather than the reference voltage itself. This integral is calculated off line and stored in a look up table in the microcomputer's memory. Also required is the integral of the boost voltage component. A compromise is chosen here. The boost voltage may change in amplitude and phase rapidly, particularly with current feedback added, making it difficult to calculate the correct third harmonic common mode voltage to be added. For this reason, no common mode component is added to the boost voltage. The error caused by this is not significant, since at high output voltages, the boost voltage component required for an induction motor is small.

5.3.4 Bank Cross-Over Technique

The bank cross-over technique used for the 3 phase cycloconverter was explained in detail in Section 3.4.

5.4 Software

For the 3 phase cycloconverter, the software was written almost entirely in the "C" programming language. This was possible because of the high processing power and

speed of the TMS320C31 processor. The complete software listing can be found in Appendix F.

The software structure is basically the same as that of the single phase cycloconverter described with flowcharts in section 4.3 and these will not be repeated here. The differences are as follows:

1. The number of samples per mains cycle has been increased from 90 to 120 to improve accuracy.

2. The software phase locked loop works as before as shown in the flowchart of Figure 4.4. The various constants are different though, to accommodate a faster clock and a higher sampling rate. the zero crossing interrupt comes from the R-S phase as shown in Figure 5.2.

3. There are three output phases, U, V, and W, instead of two, with each phase being treated separately as before.

4. The trigger periods for the different output phases no longer start at the same time. The trigger period for each phase starts at the cross-over of the voltage reference and the active input waveform as shown in Figure 3.3. The calculation of the end of the current trigger period is added to the background calculations block of Figure 4.5 for each phase.

5. The pulse input to set the speed is read by a hardware counter in the gate array rather than by an interrupt driven software counter as shown in Figure 4.5.

5.5 Tests with a Motor Load

5.5.1 Motor Characteristics

The motor used as a load is a standard TEFC two pole induction motor designed for a three phase input of 415 V at 50 Hz when connected in delta. Its name plate ratings are as follows:

Voltage: 415 V, delta connection
Frequency: 50 Hz
Current: 39 A
Speed: 2930 rpm

To match the cycloconverter, the motor was reconnected in star configuration. This changes the rated line to line voltage to 719 V at 50 Hz and 359 V at 25 Hz, which is the expected maximum frequency of the cycloconverter. This is a good match to the cycloconverter which has a maximum output of $415 \times 3/\pi = 396$ V.

The motor characteristics derived from measurements and the nameplate ratings, referred to phase to neutral with the motor connected in star, are shown in Table 5.1.

Table 5.1 Motor parameters for the three phase motor, referred to one stator winding, at a motor temperature of 20°C.

Stator Resistance, R_1	0.3 Ω
Rotor Resistance, R_2	0.5 Ω
Stator Leakage Inductance, L_1	5 mH
Rotor Leakage Inductance, L_2	5 mH
Magnetising Inductance, L_m	224 mH

The leakage inductance for this particular motor is very low, which is not ideal for the cycloconverter as it causes excessive current ripple. To compensate for this, an extra 10 mH inductor was added to each phase to lift the total leakage inductance to 20 mH.

5.5.2 Equipment Setup

For no load tests, the motor was run uncoupled. For load tests, both motoring and regenerating, the motor was coupled to a 15 kW, 1500 rpm compound DC generator, the electrical output of which was in turn connected to a motor generator set fed from the mains. This allowed the power to be recirculated to the mains. The test set-up is shown in Figure 5.6. The generator's series field was connected in reverse to normal to give the generator a very soft voltage regulation. This allowed the load to be adjusted by varying the DC bus voltage from the motor/generator set, which has a very hard regulation characteristic.

The data recording equipment used was the same as used for the single to two phase cycloconverter.

The reference flux of the cycloconverter was set to give 210 V phase to neutral at 25 Hz. This is equivalent to applying 420 V line to line at 50 Hz to the motor in its original delta configuration, which is slightly above the motor's nominal rating of 415 V. Also, a quadrature voltage boost of 3 V rms was applied to overcome the stator voltage drop due to magnetising current.

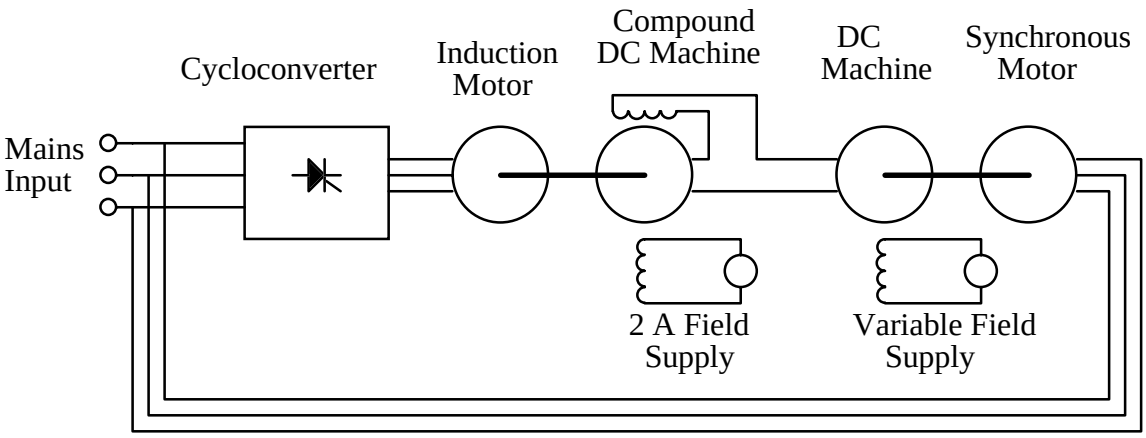


Figure 5.6 Equipment set-up for testing the 3 phase cycloconverter

5.5.3 No Load Tests

Output voltage and current waveforms for one of the three output phases were recorded at 5 Hz and 26 Hz with the motor unloaded. These waveforms are shown in Figures 5.7 and 5.8. The frequency of 26 Hz was chosen because it has no factors in common with 50 Hz allowing intermodulation products to stand out. Voltages were measured with respect to the output reference point as shown in Figure 5.2 and described in section 5.3.3.

Note the over voltage transients in both voltage waveforms. These are a result of the interaction between phases. When the phase current is zero with all thyristors off, the phase voltage is entirely dependent on the motor back e.m.f. and the voltages imposed on the other two phases. A switching transient in another phase can result in a voltage transient in the open circuit phase.

The no load current waveforms, especially at 26 Hz, are poor, but it has been found that the torque pulsations due to this are small. It is an area , though, where more work is needed. Note that the no load flux waveform at 26 Hz, as shown in Figure 5.19(a), is close to sinusoidal.

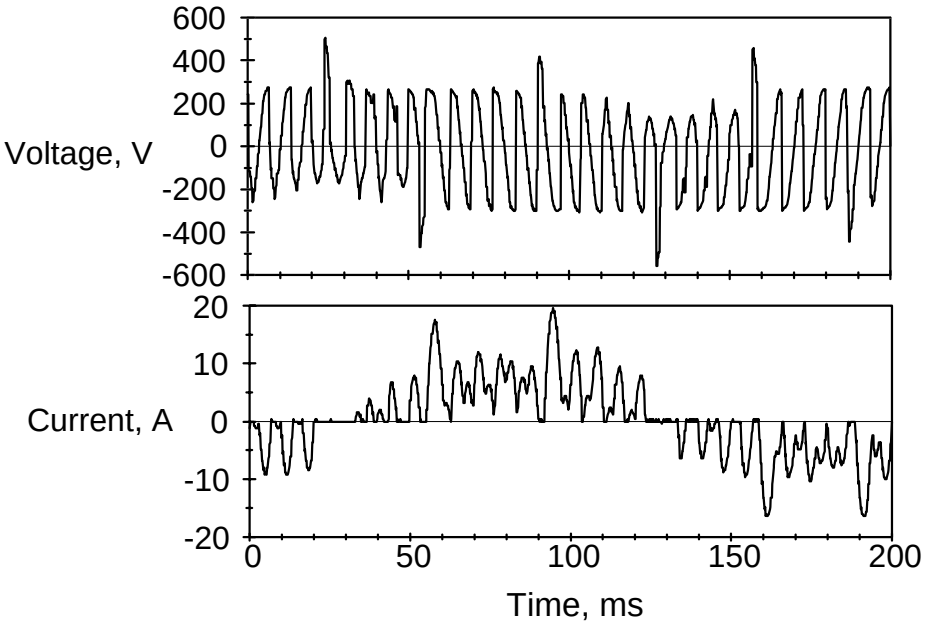


Figure 5.7 Output waveforms for the three phase cycloconverter operating at 5 Hz with no load.

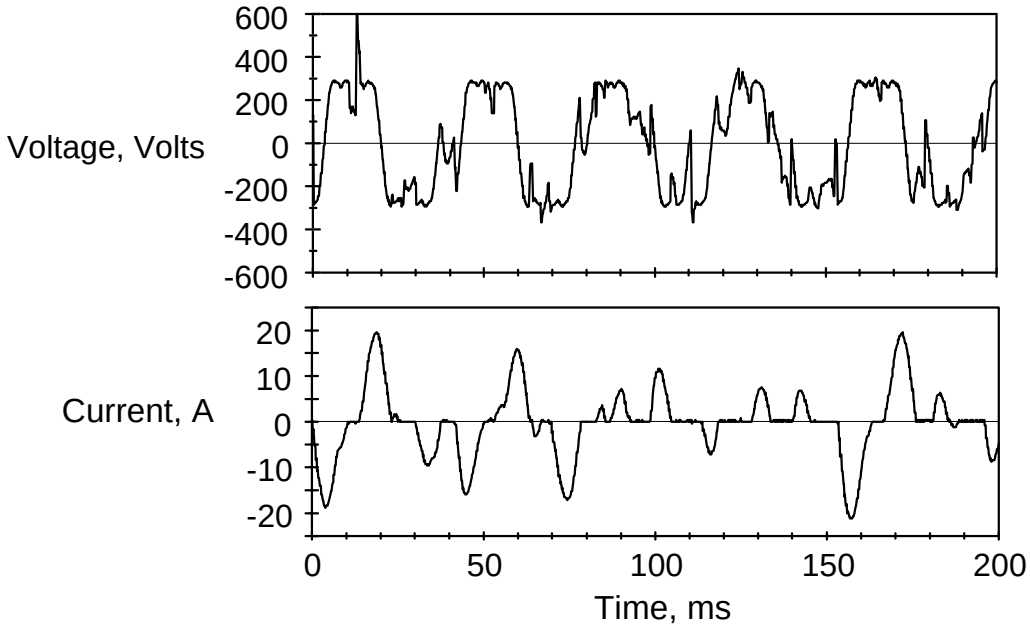


Figure 5.8 Output waveforms for the three phase cycloconverter operating at 26 Hz with no load.

5.5.4 Load Tests

The results of load tests at output frequencies of 5 Hz and 26 Hz are shown in this section. Included are output voltage waveforms for one output phase and input and output current waveforms and frequency spectra. The output voltages were measured

with respect to the output reference as for the no load tests. The motor was loaded until the motor current matched the full load rated current.

The output voltage and current waveforms at 5 Hz and full load rated current are shown in Figure 5.9. Observe that the ripple frequency of the voltage waveform is 150 Hz, but the component of the output ripple current at this frequency is suppressed to about the same level as the 300 Hz component. This is because the 150 Hz "carrier" component of the voltage is in phase on all outputs regardless of which of the negative or positive output banks is operating. This is analogous to the standard 6-pulse bridge AC to DC converter which can be thought of as two 3-pulse converters with their 150 Hz carrier components completely cancelling. Suppression of the 150 Hz component makes the output current waveform similar to that obtained from a 36 thyristor 6-pulse cycloconverter in which the carrier frequency of 300 Hz is not cancelled. The output current frequency spectrum is shown in Figure 5.10. As expected from the current waveform, the harmonics are very low.

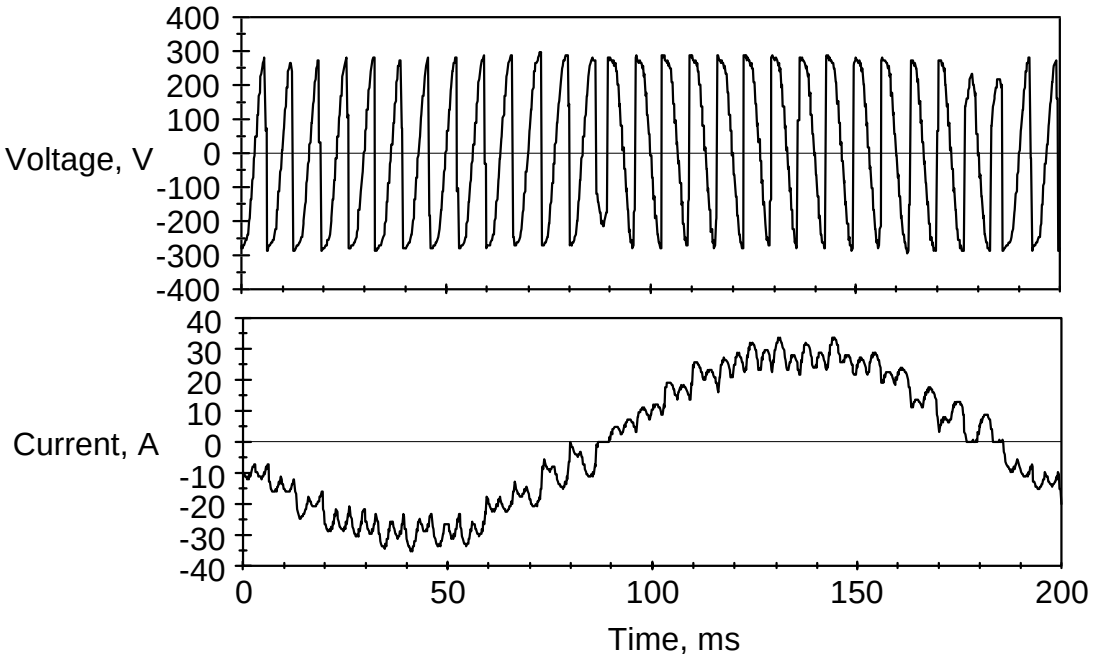


Figure 5.9 Output waveforms for the three phase cycloconverter operating at 5 Hz with a full motor load.

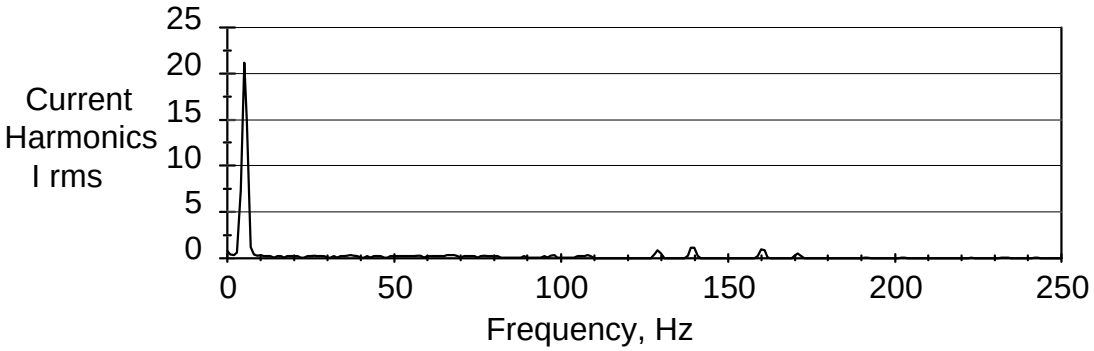


Figure 5.10 Frequency spectrum of the output current at full load with 5 Hz output frequency.

The input current waveform and its spectrum are shown in Figures 5.11 and 5.12. They are very similar to those obtained from a 6-pulse AC to DC converter or a 6-pulse three phase cycloconverter.

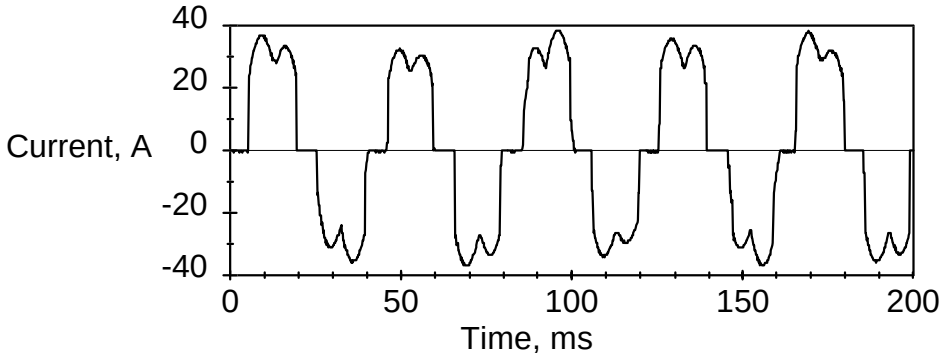


Figure 5.11 Input current waveform for the three phase cycloconverter operating at full motor load with 5 Hz output frequency.

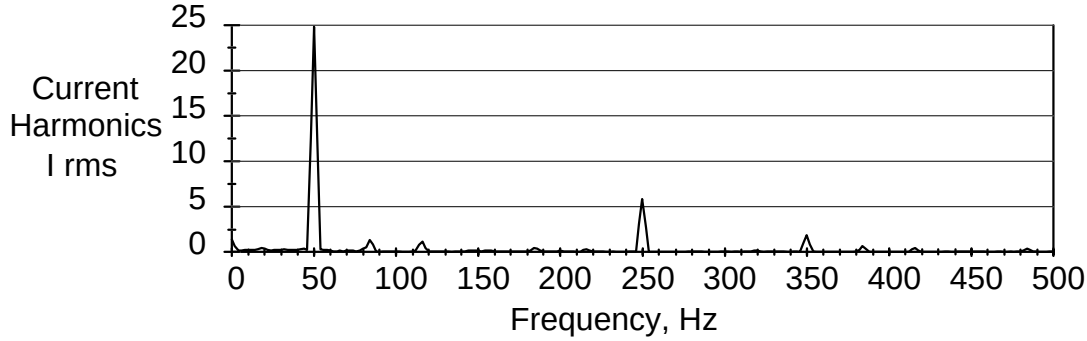


Figure 5.12 Frequency spectrum of the input current at full load with 5 Hz output frequency.

In summary, at low output voltages and frequencies, the input and output current waveforms of the 3-pulse cycloconverter with double integral control is little different from that of a 6-pulse cycloconverter.

The output voltage and current waveforms at 26 Hz which is near the upper frequency limit are shown in Figure 5.13 with the frequency spectrum of the output current shown in Figure 5.14. The intermodulation products, such as ($3f_i - 4f_o$) at 46 Hz and ($3f_i - 6f_o$) at 6 Hz, are suppressed more as their frequency drops, although the total harmonic distortion is about 40%. This increases the total rms motor current by about 8% possibly requiring a motor derating by this amount.

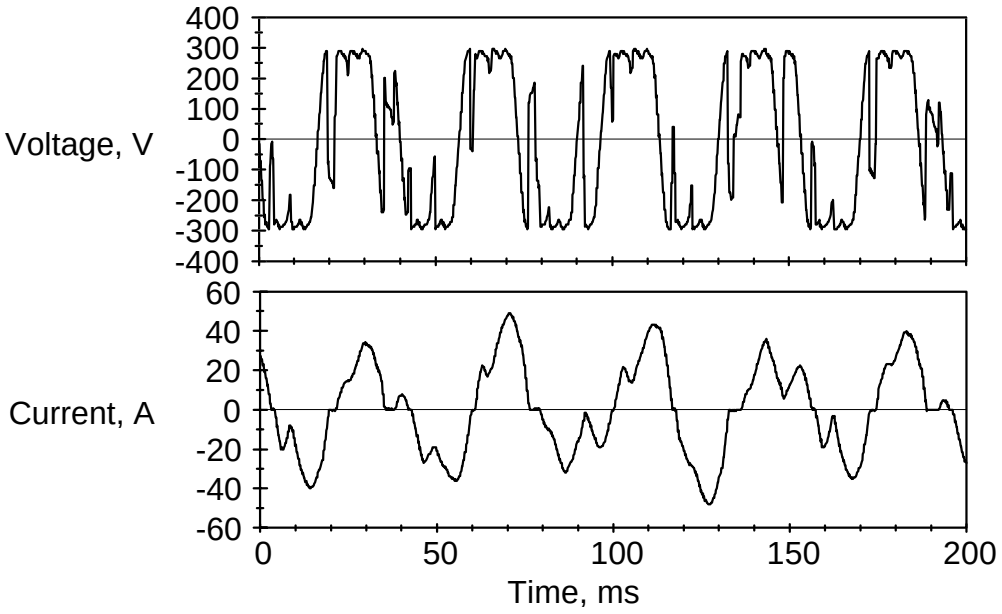


Figure 5.13 Output waveforms for the three phase cycloconverter operating at 26 Hz with a full motor load.

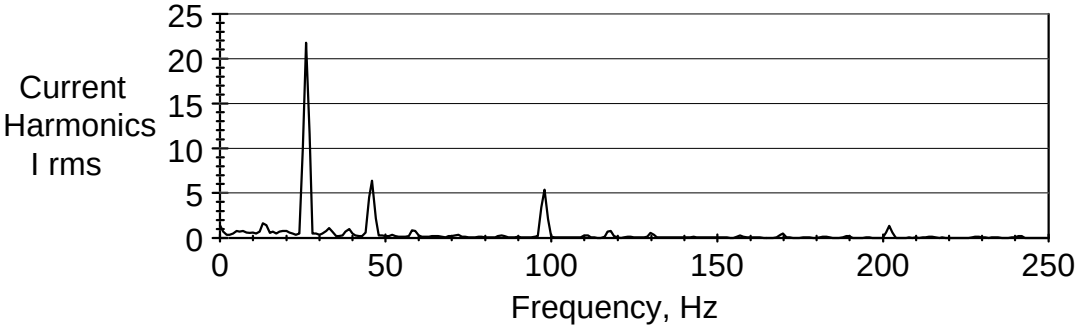


Figure 5.14 Frequency spectrum of the output current at full load with 26 Hz output frequency.

The input current and its frequency spectrum at 26 Hz are shown in Figures 5.15 and 5.16. The current waveform has only one significant frequency component apart from the 50 Hz fundamental. This is at 22 Hz and is actually the $(2f_i - 3f_o)$ intermodulation product. This may present a problem for some supply systems. It may be possible to reduce the magnitude of this component by adjustment to the phase control. This would probably also improve the output waveforms as the power flow from input to output would be more even.

As the output frequency increases above 26 Hz, the input $(2f_i - 3f_o)$ subharmonic drops lower in frequency and grows in amplitude, becoming DC at 33 Hz. Also, the total harmonic distortion on the output rises rapidly at frequencies above 26 Hz. Even so, full load operation to at least 30 Hz is possible if required.

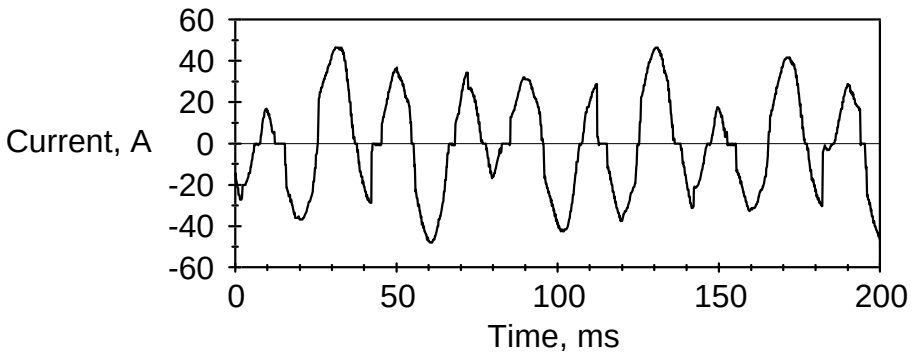


Figure 5.15 Input current waveform for the three phase cycloconverter operating at full motor load with 26 Hz output frequency.

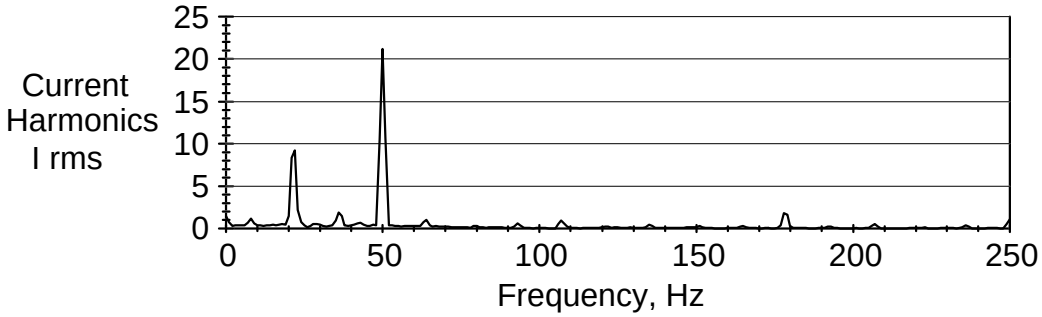


Figure 5.16 Frequency spectrum of the input current at full load with 26 Hz output frequency.

5.5.5 Regenerative Load Tests

As expected, the performance with a regenerative load was found to be similar to the performance with a motoring load. The voltage and current waveforms near full

regeneration at 22 Hz output frequency are shown in Figure 5.17. They are similar to the corresponding motoring waveforms.

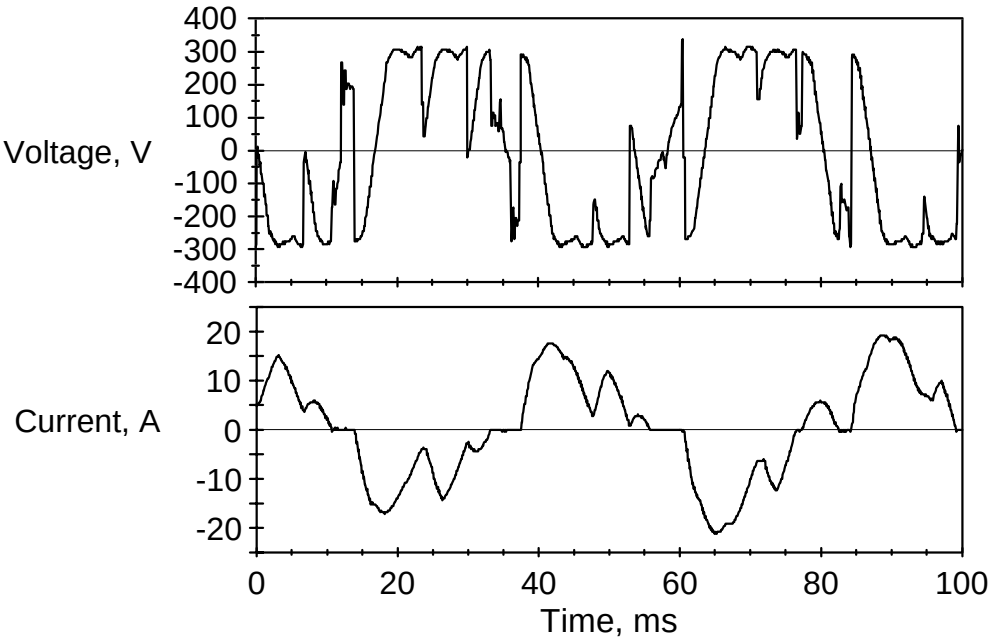


Figure 5.17 Output waveforms for the three phase cycloconverter operating at 22 Hz with a regenerative load.

5.5.6 Feedback Flux Waveforms

The reference and feedback flux waveforms as obtained directly from the microcomputer at 20 and 26 Hz and at no load and full load are shown in Figures 5.18 and 5.19. Note that the reference flux waveform is not quite sinusoidal. It is the integral of the required output voltage waveform shown in Figure 5.5(c). The double integral control keeps the feedback waveform very close to the reference, although the error increases under load and also at higher frequencies.

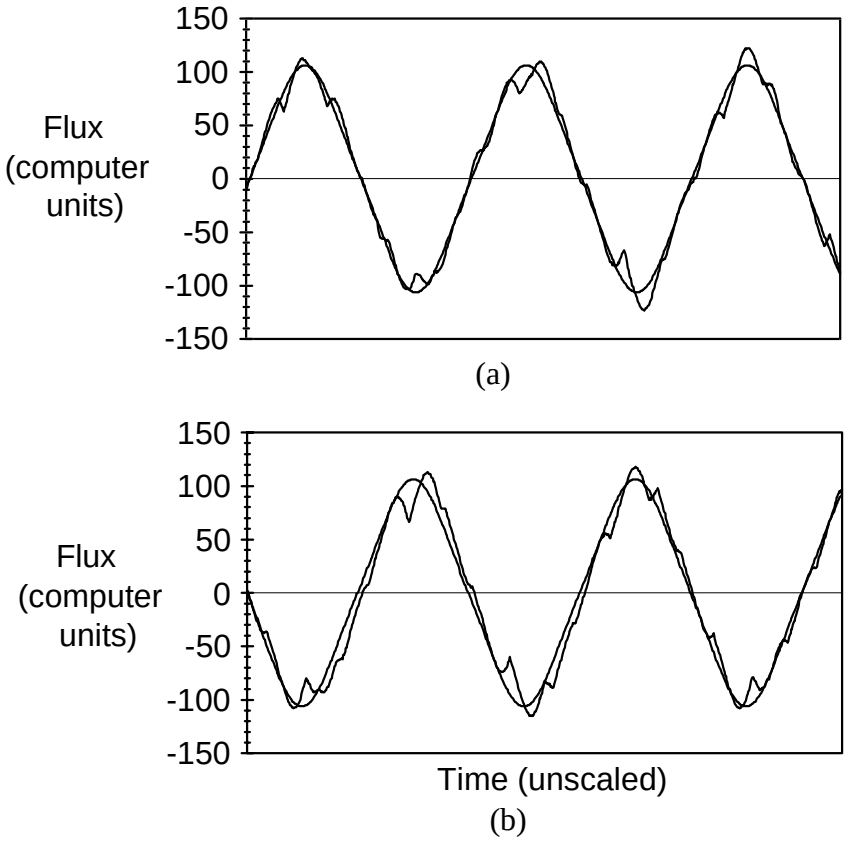


Figure 5.18 Feedback and reference flux waveforms at 20 Hz at (a) no load, (b) full load.

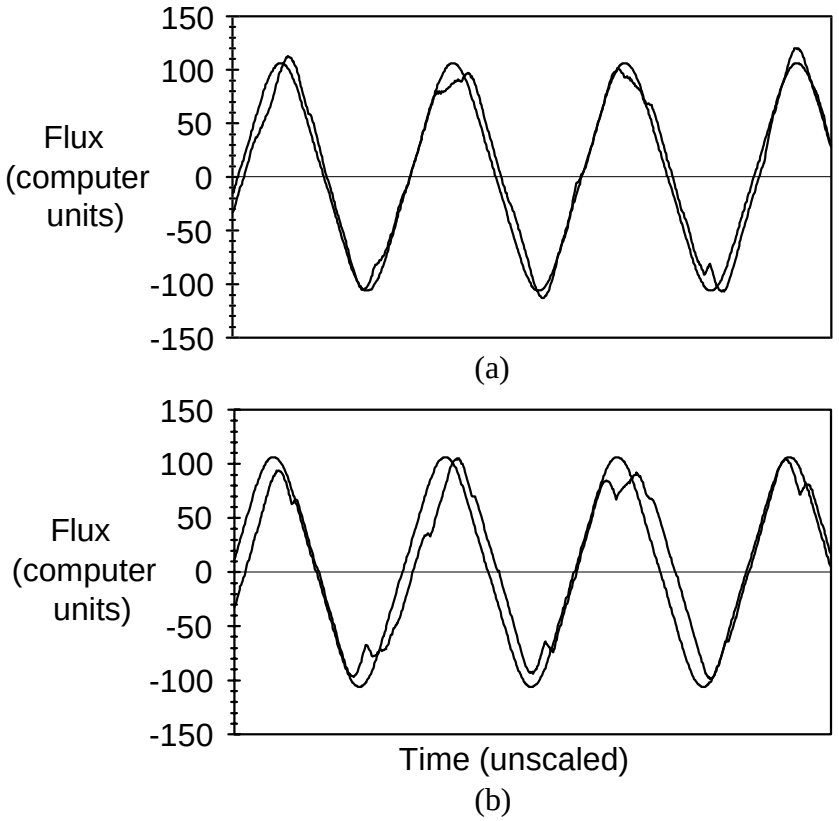


Figure 5.19 Feedback and reference flux waveforms at 26 Hz at (a) no load, (b) full load.

6. CONCLUSION

Cycloconverters have been in use since the 1930's and they are the first fully static AC variable voltage variable frequency drives to be used. In recent years, they have found extensive use as high power, high performance AC drives particularly in cement mills and rolling mills.

All current commercial cycloconverter drives use pulse numbers of 6 or higher. With traditional phase control techniques, cycloconverters of lower pulse number cannot be used as motor drives because of their high level of output subharmonics and their difficulty in handling bank crossover and discontinuous currents. In cycloconverters of higher pulse numbers, these problems have been traditionally suppressed by the use of current feedback. Stability limits prevent its use, though, with lower pulse number cycloconverters. The problems with low pulse number cycloconverters, particularly subharmonic production, have remained unsolved for such a long time that many drive designers consider them to be inherent unavoidable characteristics of these drives.

This thesis introduced a new modulation technique called double integral control which, using a combination of feed forward and feed back techniques, forces the motor flux, measured by the feedback of the integral of the motor voltage, to follow a reference flux. This new control method inherently suppresses all subharmonics. It also automatically corrects for discontinuous current and allows accurate selection of the optimum bank cross-over time. Its dynamic response allows operation of the cycloconverter to much higher frequencies then were previously thought possible.

Two cycloconverter induction motor drives using the new modulation technique were presented. The first is a new single phase to two phase cycloconverter motor drive which uses split phase motor windings and only four triacs, all of which are connected to the neutral allowing non-isolated gate drive. The drive has very low cost and can operate in all four quadrants up to 20 Hz. The drive also generates low e.m.i. and has very low input current distortion, easily meeting all international standards for mains distortion.

The second drive is a standard three phase drive with a 3-pulse, three phase cycloconverter using 18 thyristors. With double integral control, it can operate in all four quadrants at full load up to 30 Hz output frequency. At low output frequencies, input and output current waveforms are similar to 6-pulse cycloconverters, with the 3-pulse derived harmonics being cancelled out. Input and output harmonics increase with

output frequency and voltage, with output current distortion reaching 40% at 26 Hz, requiring a 10% motor derating at this frequency. Subharmonic components are completely suppressed at all frequencies. The limited output frequency is not a major deficiency, since with a two pole motor, it can achieve the industry standard 0-1500 rpm speed range. With its rugged thyristor power circuit, low cost, low input harmonics, and four quadrant operation, this drive should become a standard drive in industry.

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Publications Derived from this Thesis:

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APPENDIX A: Derivation of formulae used in the simulation of the 2-pulse cycloconverter for determining the optimum value of the stability constant, *K*

For the waveforms shown in figure 3.5, equation 3.3 can be expanded as follows:

$$
\begin{aligned}
0 &= \int_0^{\pi}\int^{t} v_o dt^2 + K\pi\int_0^{\pi} v_o dt \\
&= \pi\int^{0} v_o dt + \int_0^{\pi}\int_0^{t} v_o dt^2 + K\pi\int_0^{\pi} v_o dt \\
&= \pi\int^{0} v_o dt + \int_0^{t_f}\int_0^{t} v_o dt^2 + \int_{t_f}^{\pi}\left(\int_0^{t_f} v_o dt + \int_{t_f}^{t} v_o dt\right)dt + K\pi_f\left(\int_0^{t_f} v_o dt + \int_{t_f}^{\pi} v_o dt\right) \\
&= \pi\int^{0} v_o dt + \int_0^{t_f}\int_0^{t} v_o dt^2 + \left(\pi - t_f\right)\int_0^{t_f} v_o dt + \int_{t_f}^{\pi}\int_{t_f}^{t} v_o dt^2 + K\pi\left(\int_0^{t_f} v_o dt + \int_{t_f}^{\pi} v_o dt\right) \\
&= \pi\int^{0} v_o dt + \int_0^{t_f}\int_0^{t} v_o dt^2 + \left(K\pi + \pi - t_f\right)\int_0^{t_f} v_o dt + \int_{t_f}^{\pi}\int_{t_f}^{t} v_o dt^2 + K\pi\int_{t_f}^{\pi} v_o dt \\
&= \pi\int^{0} v_o dt + \int_0^{t_f}\int_0^{t} -\sin t dt^2 + \left(K\pi + \pi - t_f\right)\int_0^{t_f} -\sin t dt + \int_{t_f}^{\pi}\int_{t_f}^{t} \sin t dt^2 + K\pi\int_{t_f}^{\pi}\sin t dt \\
&= \pi\int^{0} v_o dt + \int_0^{t_f}(\cos t - 1)dt + \left(K\pi + \pi - t_f\right)\int_0^{t_f} -\sin t dt + \int_{t_f}^{\pi}\left(\cos t_f - \cos t\right)dt + K\pi\int_{t_f}^{\pi}\sin t dt \\
&= \pi\int^{0} v_o dt + \sin t_f - t_f + \left(K\pi + \pi - t_f\right)\left(\cos t_f - 1\right) + \left(\pi - t_f\right)\cos t_f + \sin t_f + K\pi\left(1 + \cos t_f\right) \\
&= \pi\int^{0} v_o dt + 2\sin t_f + 2\left(K\pi + \pi - t_f\right)\cos t_f - \pi
\end{aligned}
$$

Also, equation 3.5 is derived as follows:

$$
\begin{aligned}
\int_{t_f}^{\pi} v_o dt &= \int^{0} v_o dt + \int_0^{t_f} v_o dt + \int_{t_f}^{\pi} v_o dt \\
&= \int^{0} v_o dt + \int_0^{t_f} -\sin t dt + \int_{t_f}^{\pi}\sin t dt \\
&= \int^{0} v_o dt + \cos t_f - 1 + 1 + \cos t_f \\
&= \int^{0} v_o dt + 2\cos t_f
\end{aligned}
$$

APPENDIX B: Circuit schematic diagrams for the single phase to two phase cycloconverter

APPENDIX C: Software listing for the single phase to two phase cycloconverter

The software is for the TMS320E14 digital signal processor and is written in assembler. For a guide to the pseudo code documentation, see Appendix G.

The following equation (from equation 3.23) is used as the double integral algorithm in the software. The terms are labelled for identification.

$$0 = -\int_{t_1}^{t_2} \psi(t)dt - K(t_2 - t_1)\left[\psi(t_2) - \psi(t_1)\right]$$

1(a) 1(b)

$$-K(t_2 - t_1)\int^{t_1} v_o' dt$$

2

$$+\int_{t_1}^{t_f}\int^{t} v_o' dt^2 + (t_2 - t_f)\int^{t_f} v_o' dt + K(t_2 - t_1)\int^{t_f} v_o' dt$$

3 4(a) 4(b)

$$+\int_{t_f}^{t_2}\int_{t_f}^{t} v_t dt^2 + K(t_2 - t_1)\int_{t_f}^{t_2} v_t dt$$

4(c) 4(d)

APPENDIX D: Circuit schematic diagrams for the control circuit of the three phase cycloconverter

APPENDIX E: Gate array logic diagrams for the three phase cycloconverter

The SERIAL and the TACHO blocks are included or future expansion. No peripherals as yet are attached to these blocks.

Note that some diagrams extend over two pages.

APPENDIX F: Software listing for the three phase cycloconverter

The software is written mostly in the C programming language with some routines written in assembler language for the TMS320C31 digital signal processor. For a guide to the pseudo code documentation, see Appendix G.

The following equation (from equation 3.17) is used as the double integral algorithm in the software. The terms are labelled for identification.

$$0 = \underbrace{\int_{t_0}^{t_2}\int_{t_0}^{t} v_t dt^2}_{1(a)} + \underbrace{K(t_2 - t_1)\int_{t_0}^{t_2} v_t dt}_{1(c)}$$

$$\underbrace{-\int_{t_1}^{t_2}\int_{t_1}^{t} v_b dt^2}_{1(e)} - \underbrace{K(t_2 - t_1)\int_{t_1}^{t_2} v_b dt}_{1(f)}$$

$$\underbrace{-\int_{t_1}^{t_2} \psi(t) dt}_{1(b)} - \underbrace{K(t_2 - t_1)\left[\psi(t_2) - \psi(t_1)\right]}_{1(d)}$$

$$-K(t_2 - t_1)\int^{t_1} (v_o - v_b) dt$$

2

$$\underbrace{+\int_{t_1}^{t_f}\int^{t} (v_o - v_b) dt^2}_{3(a)} + \underbrace{(t_2 - t_f)\int^{t_f} (v_o - v_b) dt}_{4(a)} + \underbrace{K(t_2 - t_1)\int^{t_f} (v_o - v_b) dt}_{4(b)}$$

$$\underbrace{-\int_{t_0}^{t_f}\int_{t_0}^{t} v_t dt^2}_{3(b)} - \underbrace{(t_2 - t_f)\int_{t_0}^{t_f} v_t dt}_{4(c)} - \underbrace{K(t_2 - t_1)\int_{t_0}^{t_f} v_t dt}_{4(d)}$$

$$\underbrace{+\int_{t_1}^{t_f}\int_{t_1}^{t} v_b dt^2}_{3(c)} + \underbrace{(t_2 - t_f)\int_{t_1}^{t_f} v_b dt}_{4(e)} + \underbrace{K(t_2 - t_1)\int_{t_1}^{t_f} v_b dt}_{4(f)}$$

APPENDIX G: A guide to software documentation

Introduction

This document describes a standard procedure for designing and documenting assembler language programs. It covers the main body of the program only. It does not cover other aspects of documenting a program such as variable listings and descriptions and program headings and descriptions. It can also be used for writing and documenting high level languages such as "C". Such a standard is needed so that all programs have consistency in documentation methods and programming methods independent of who wrote the programs. The aim of the standard is to make it as easy as possible for programs to be understood and modified after they have been written, even if the original programmer is no longer available.

The design and documentation procedure is described below.

Program Documentation

The documentation for each line or group of lines of code is written on a separate line above where the code is to be written. This is formatted as shown later to show the program structure.

This has two advantages. First, it allows the programmer to write the documentation first and then the code. Using the documentation to write the code helps ensure that the documentation is adequate and allows the program structure and logic to be checked before coding. Second, it eases the job of transferring the program to another microprocessor or language, which invariably occurs during the life of the program. The code can be deleted and rewritten while leaving the documentation intact.

Program Structuring

The method of structuring a program is described below and is based on the work of Jean-Dominique Warnier [see reference]. This work in turn is based on set theory, giving it a good mathematical foundation. This derivation from set theory shows itself in the use of set theory notation to indicate program structure instead of the more usual IF - THEN - ELSE or REPEAT - UNTIL type notation. The set theory notation has the advantages of more clearly showing the program structure and of brevity.

The program is divided into sequential sections. Each section is headed by a line of documentation describing the section. Each of these sections is then treated as a program in its own right which is again divided into sections. Each section is indented from its parent section to show structure. Alternatively, a section is expanded as a separate sub-program in another module. This hierarchical process of dividing each section into further self contained sections is continued until each section heading is simple enough to form the documentation for a line or group of lines of code. The code is then written for each unexpanded section.

The program control structure - loops and conditional branching - is created by allowing a section to either run or not run, or to repeat a certain number of times during program execution. Only four possibilities are allowed:

1. A section always runs once during program execution. This is the default section type and no notation is required to indicate it. Such a section can be optionally denoted by putting '(1 times)' at the end of the section heading.

2. A section runs 0 or 1 times during program execution in mutual exclusion to a second section running 1 or 0 times. The two sections of this mutually exclusive pair are placed one after another in the program. The first section is denoted with '(0,1)#' placed after the section heading and the second section of the pair is denoted with '#(0,1)'. the '#' symbol is used to represent 'exclusive or'. This structure is equivalent to the IF .. THEN .. ELSE .. structure in Basic.

   Quite often, one of the mutually exclusive sections does nothing. A short-hand method of documenting this situation is to leave out the section that does nothing altogether and denote the remaining section with just '(0,1)'. This is equivalent to removing the ELSE part of an IF .. THEN .. ELSE .. structure in Basic. In this situation, the alternate section is still there, but is implied. Quite often during later program modification this section has to be re-inserted.

   The mutually exclusive pair of sections is usually proceeded by a section of type (1 times) which does the testing and branching. This is the IF .. part of the IF .. THEN .. ELSE .. structure.

3. A section is repeated a fixed number of times (more than once) during program execution. Such a section is denoted by putting '(n times)' at the end of the section heading where n is the number of times it is repeated. This structure is equivalent to the FOR loop in Basic.

4. A section is repeated a variable number of times greater than or equal to once for different program runs. Such a section is denoted by putting '(1,n)' at the end of the section heading where n is the maximum number of times it is repeated. If n is unknown, the notation'(1,.)' or '(1,?)' can be used. This structure is similar to the REPEAT ... UNTIL loop in Pascal.

Program Flow

Within a program (which also means within a section or sub-section), the program flow is always from top to bottom, with the exception that conditional sections, i.e. sections of type (0,1), (0,1)#, or #(0,1), may be skipped over.

Rules on Exiting from a Section

There should only be one exit point for a section and this is the last sub-section. This means that the last sub-section cannot be part of an exclusive or pair. This may entail adding a dummy 'end' sub-section - see Example 1 in the Appendix.

If execution speed has absolute priority over ease of maintenance, this may be relaxed by allowing exit from either one of an exclusive or pair if these appear last in a section.

Subroutines

Subroutines may be used with the above structure in two ways. First, any section may be made into a subroutine. This results in the program being split into hierarchical modules and is to be encouraged. Second, when two or more sub-sections appearing under different sections do the same thing, each sub-section may call a common subroutine to save duplicating code.

Other Program Structures

Other program structures are allowed in many high level languages which are disallowed in this standard.

One structure in particular which is used extensively in high level languages which is not allowed here is the WHILE loop. Using the above notation, this could be called a (0,n) type structure. It is a repeated loop which may also not run at all. It is shown by Warnier that it is much better to separate this structure into a (1,n) type structure inside a

(0,1) type structure. He shows that splitting the WHILE loop into these two structures makes it much easier to optimise the program structure for speed and size. Another reason for splitting the WHILE loop structure is that most assembler languages do not support it - it usually has to be implemented by splitting it into a (0,1) and a (1,n) structure anyway. Yet another reason is that a (0,1) section is always mutually exclusive to another implied (0,1) section which does nothing. During later maintenance, this implied section may have to be brought into being and code added.

Another common structure in high level languages consists of a set of three or more sections in which only one runs during program execution. An example is the CASE statement in Pascal. This structure is not normally allowed in this standard and should be replaced with nested mutually exclusive pairs. The exception is that some microcomputers have a computed GOTO or indirect branch instruction built in which can save considerable execution time over using nested mutually exclusive pairs in some instances. The computed GOTO, though, should be used with caution and only when needed.

Program Flow Charting

With the above program structures, flow charting is not required. The program flow within each program or section is always from start to finish with the exception of repeat loops only.

A good test to see if the above rules have been adhered to is that if all the code lines, address pointers and labels are removed from the program, the documentation shows exactly what the program does and how the program flows (i.e. how it is structured).

Reference

Jean-Dominique Warnier: "Logical Construction of Programs" H.E. Stenfert Kroese B.V. - Leiden.